1/f Noise Characterization of a Surface-Micromachined Suspended Gate FET

Hua Fu, Margaret L. Kniffin, Glenn Watanabe, Michael P. Masquelier, James Whitfield

Abstract—**This paper presents the first detailed characterization and modeling of 1/f noise in a depletion mode surface-micromachined suspended gate nMOSFET. The results are compared and contrasted with the 1/f noise characteristics of a standard depletion mode nMOSFET. Due to the depletion mode nature of both surface-micromachined suspended gate FET and standard FET, 1/f noise decreases as the gate bias approaches to the threshold voltage. 1/f noise component can be modeled using the standard SPICE type of equation. The derived model can be used directly in the optimization of suspended gate transducer design.**

Index terms— **1/f noise, depletion mode NMOS, surface-micromachined suspended gate FET**

I. Introduction

First proposed by Nathanson et. al. [1], suspended gate FETs have been used in the design of numerous types of MEMs transducers. These include microphones, pressure sensors, accelerometers and CHEMFET sensor [2-5]. For many applications the frequencies of interest are in the <1000 Hz range, which means that MOSFET flicker noise can play a significant role in determining the fundamental performance limit of the transducer. Despite its importance, little information on the noise performance of suspended gate MOSFETs has been reported in the literature. In this paper, we present the first detailed characterization and modeling of flicker noise in a depletion mode surface-micromachined suspended gate nMOSFET. These results are compared and contrasted with the low frequency noise characteristics of a standard depletion mode nMOSFET. SPICE 1/f noise equation is used to model the measurement results. The derived model can be used directly in the optimization of suspended gate transducer design.

II. Device Description

The depletion mode suspended gate FETs were fabricated using an interleaved process which combines polysilicon surface micromachining techniques with a conventional enhancement-depletion NMOS process flow. This is a 13 mask process with the MOSFETs and transducer sharing many common process modules, including a single 1μm polysilicon layer which is used to form both the suspended and standard gate electrodes. The test structure consists of an array of suspended polysilicon fingers which are attached to a rectangular anchor which is affixed to the substrate. A SEM micrograph of an array of suspended gate FET fingers is shown in figure 1. The suspended fingers form the gate of a series of depletion-mode FETs patterned in the underlying substrate. The regions in between gate fingers are the sources and drains of the devices. A buried channel is formed by implanting substrate with arsenic prior to polygate deposition and subsequent high temperature anneal to relieve the stress in the polysilicon.

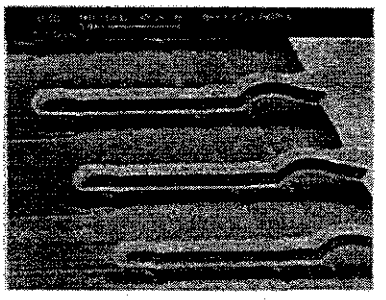

Figure 1. A SEM micrograph of a test array of surface micromachined suspended gate FETs.

III. Measurement Results and Discussion

A suspended gate depletion mode FET (drawn W/L=9μm/5μm) and a standard depletion mode FET (drawn W/L=100μm/5μm) were tested. The DC characteristics of both devices are shown in Figure 2. Open circles are the bias points for 1/f noise measurement. The threshold voltage of the standard depletion mode FET is -0.91V and that of the suspended gate FET is -10.95V. Larger negative threshold voltage of the suspended gate FET is due to the larger equivalent oxide thickness.

1/f noise was measured as a function of both gate and drain bias with an HP3561 spectrum analyzer and the input-referred noise voltage spectral density was calculated from the data based on a small signal circuit model[7].

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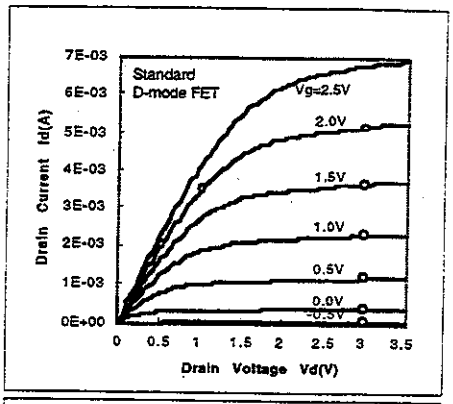

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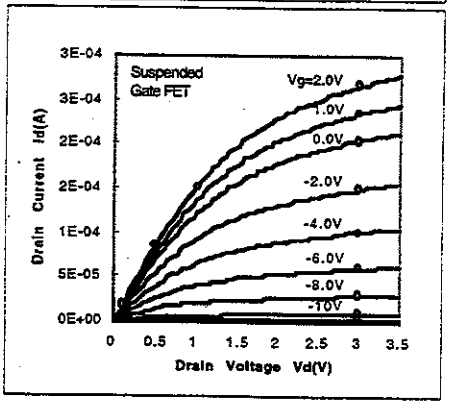

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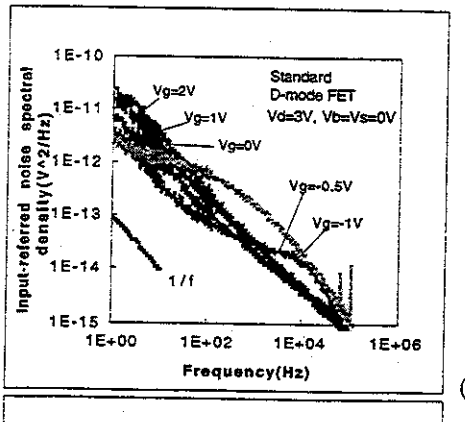
Figure 2. Output characteristics of (a) a standard and (b) a suspended gate depletion mode nMOSFET.



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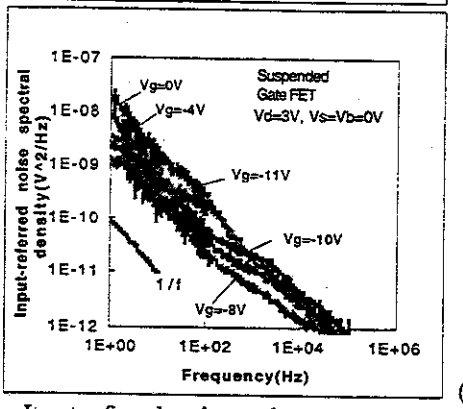
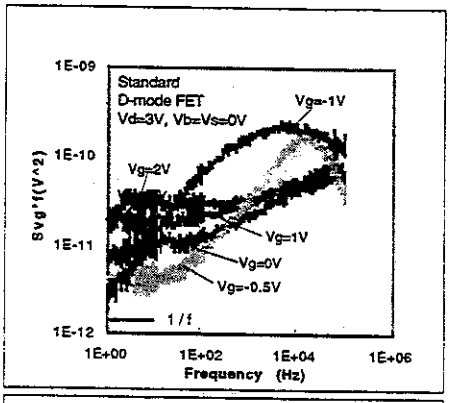


(b)

Figure 3. Input-referred noise voltage spectral density as function of gate bias for (a) a standard and (b) a suspended gate depletion mode MOSFET.

In Figure 3, the input-referred noise voltage spectral density is plotted as function of gate bias for the two devices. In both cases the low frequency spectrum exhibit pure 1/f slope for most gate biases. At gate biases greater than 2V, the input referred noise spectral density is independent of gate voltage. As the gate voltage passes through zero, the low frequency 1/f component of the noise spectrum for the standard MOSFET starts to decrease and is reduced by almost an order of magnitude near threshold. This behavior is typical of buried channel MOSFETs and can be understood by considering how the spatial distribution of carriers changes as a function of gate bias[6]. As gate bias decreases towards threshold voltage, the conducting channel is moving away from the Si/SiO_2 interface traps. The fluctuation of the channel carrier density is affected less by the interface, therefore, the 1/f noise is reduced. For the suspended gate FET a similar trend is observed.

At biases close to threshold, a significant amount of bias dependent generation-recombination (G/R) noise is present. The superposition of G/R noise on 1/f noise can be seen clearly in figure 4 where the product of the input-referred noise voltage and frequency has been plotted as function of frequency for the two devices. The Lorentzian shaped hump comes from generation-recombination noise. The peak frequency is the inverse of the time constant of the G/R center. In the standard depletion mode MOSFET, G/R with a single time constant is observed. The G/R time constant increases as gate bias moves to very close to the



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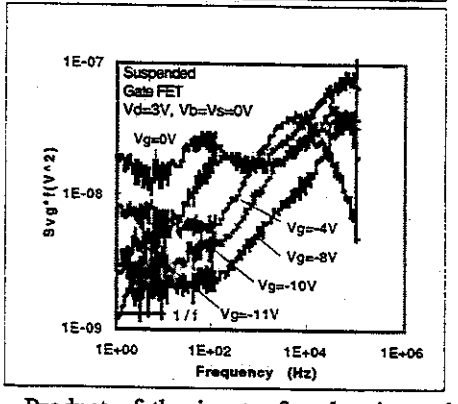


(b)

Figure 4. Product of the input-referred noise voltage and frequency (S_{vg} (f)*f) as function of frequency for (a) a standard and (b) a suspended gate depletion mode MOSFET. Vd=3V for both cases.

threshold. As a result, low frequency noise is increased and deviates from 1/f relationship.

In the suspended gate FET, situation is a little more complicated, as shown in Figure 4(b). It appears that there are two G/R centers with different time constants. The two time constants of the R/G centers decrease as the gate bias decreases(humps moving towards high frequency), therefore, do not interfere with 1/f noise component, but time constants then increase (humps moving towards low frequency), and cause increase of apparent 1/f component near threshold. The cause and location of these G/R centers need further investigation.

In Figure 5, the input-referred noise voltage spectral density is plotted as function of drain bias for the two devices. Gate voltage is fixed at 2V. In the case of standard FET, there is strong drain bias dependency. In the case of suspended gate, dependency on the drain bias is weak.

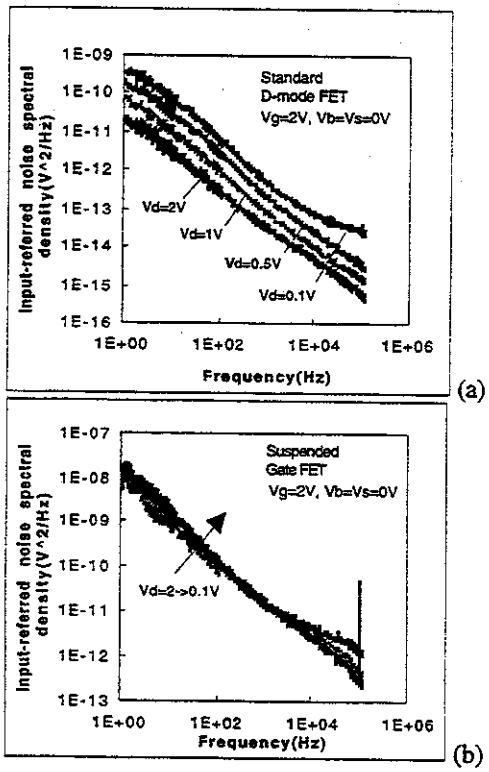


Figure 5. Input-referred noise voltage spectral density as function of drain bias for (a) a standard and (b) a suspended gate depletion mode nMOSFET. The gate voltage is fixed at 2V.

IV. 1/F NOISE MODELING

As shown in Figures 4 and 5, the input referred noise spectrum follow the 1/f relationship for frequency less than 1000 Hz when devices are biased above threshold. Also, the 1/f noise spectrum at low frequency have both gate and drain voltage dependency. This dependency can be fairly adequately modeled using a level 0 SPICE noise model.

For this model, the noise current spectral density can be fitted by the following equation:

$$\frac{\overline{i_f^2}}{\Delta f} = \frac{KF \cdot I_D^{AF}}{C_{ox}^{CEXP} \cdot L_{eff}^2} \frac{1}{f^{FEXP}} \qquad (1)$$

where i_f is the noise current at the drain of the FET, C_{ox} the equivalent oxide capacitance, I_D the DC drain current, and L_{eff} the effective channel length of the FET. *KF*, *AF*, *CEXP* and *FEXP* are the fitting parameters for 1/f noise spectrum. The same model parameters (*KF*=8.98e-26, *CEXP*=0.95, *FEXP*=1 and *AF*=1.92) and same L_{eff} values were used to fit both devices, suggesting that additional processing associated with forming a surface-micromachined suspended gate has little impact on the quality of the silicon dioxide-silicon interface. Figure 6 shows the comparison of measured and simulated (using level 0 SPICE noise model) gate bias dependent drain noise current at 1Hz for both devices. The drain bias is fixed at 3V. The simulation matches the measured dependence on the gate voltage fairly well for both devices, however it overpredicts the drain bias dependent noise for the suspended gate FET. The discontinuity seen in the data in Fig. 6 at positive gate biases is related to the formation of a depletion region at the buried channel surface. The SPICE model shown in Eqn (1) is not specifically derived for a buried channel FET, thus does not accurately account for this transition. Figure 7 shows the comparison of measured and simulated (using level 0 SPICE noise model) drain bias dependent drain

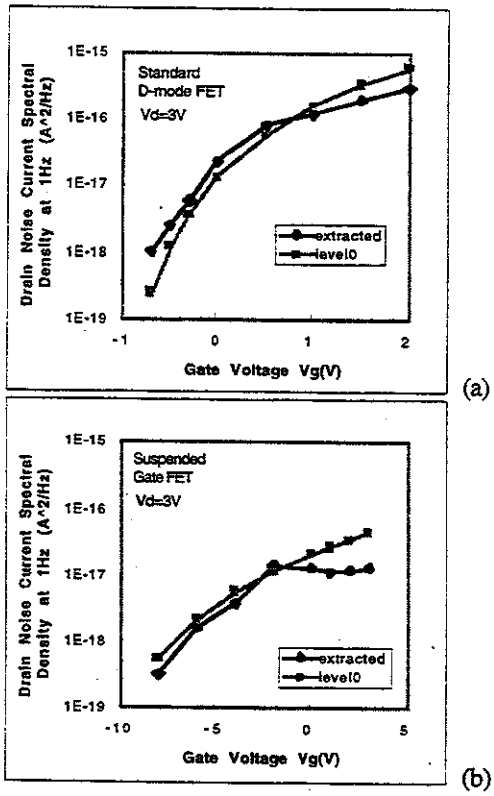
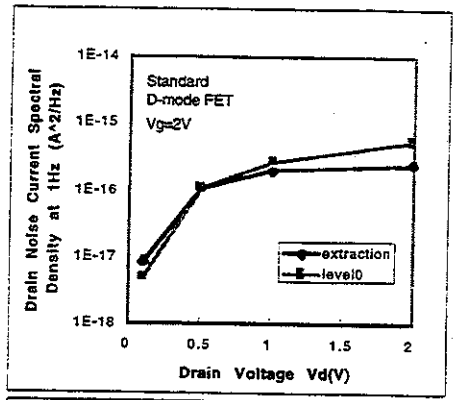


Figure 6. Comparison of measured and simulated gate bias dependent drain noise current at 1Hz for (a) a standard and (b) a suspended gate FET. The drain voltage was fixed at 3 volts.

noise current at 1Hz for both devices. The gate bias is fixed at 3V. While the model predicts the drain bias dependency of standard FET fairly well, it over predicts the noise for suspended gate FET.



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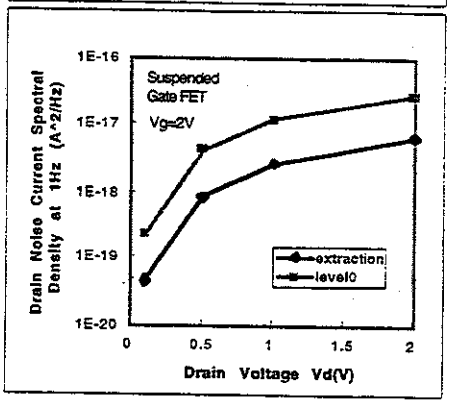

(b)

Figure 7. Comparison of measured and drain bias dependent drain noise current at 1Hz for (a) a standard and (b) a suspended gate FET. The gate voltage was fixed at 2 volts.

V. Conclusion

We have shown that the low frequency noise performance of a suspended gate depletion mode FET is mainly dominated by 1/f noise and that it can be adequately modeled using standard noise equations. For biases where G/R noise is absent, the output noise current can be calculated by integrating the noise equation over the appropriate frequency range and used to predict the signal-to-noise performance of a given suspended gate transducer design. For this particular suspended gate transistor the worst case integrated noise current over a 1000 Hz bandwidth is on the order of 15 nA.

VI. Aknowledgement

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