Automatic generation of RF compact models from device simulation

S. Luryi and A. Pacelli
Department of Electrical and Computer Engineering
State University of New York, Stony Brook, NY 11794-2350, (serge,pacelli)@ece.sunysb.edu

ABSTRACT

We review a recently proposed methodology for automatic generation of equivalent circuits from physical device simulation. The method is based on the calibration on a simplified equivalent-circuit model on simulation results, and can achieve an optimum balance of model complexity, accuracy, and generality. We discuss some of the possible applications of the technique to the modeling of active devices, parasitic elements, and complex physical effects such as self-heating and hot-carrier transport.

Keywords: Compact models; device simulation; RF; interconnects; self-heating

1 INTRODUCTION

Conventional RF modeling of device behavior is done by fitting parameters of a pre-conceived model of a given device (e.g, the Gummel-Poon model of a bipolar transistor) to empirical dc and ac data (e.g, Gummel plots and scattering parameters). This approach fails in at least three situations:

1. When one deals with a new type of device for which the device physicists have not done their homework;
2. When miniaturization of standard devices brings about new phenomena not accounted for by the pre-conceived model; this situation is all too familiar and ranges from short-channel effects in a single MOS transistor to mutual interference between several closely spaced devices to effects of packaging and environment;
3. When the device operation is stretched into a new regime, where the old pre-conceived model does not work; this situation includes high-power and/or high-frequency operation, operation in an unusual physical environment, such as magnetic field, incident radiation, etc.

Modern device modeling codes enable the designer to simulate the behavior of nearly arbitrary three-dimensional semiconductor device structures with multiple electrodes. The result can be employed to develop an equivalent circuit, but the way this is done conventionally is by simply using the simulator as a convenient "experiment in the bottle." This procedure may be even more convenient than an actual experiment, since it makes clear what is and what is not included in the device behavior. However, the choice of the equivalent circuit topology still requires an expert guess. Clearly, this procedure suffers from the same limitations as fitting to experiment.

Here we discuss a different approach to the problem, based on physical device modeling without any pre-conceived circuit topology. Ultimately, we would like to automate the choice of topology itself. If the choice is made right, parameter calibration should be a routine procedure. As we will see, the approach is quite general, and can be applied to areas well beyond semiconductor device modeling, such as interconnection networks and heat-transport effects.

A device modeling code solves the semiconductor transport equations together with Poisson's equation, and produces files that describe all the internal fields in the device, i.e., the electrostatic potential, carrier concentrations, and possibly the effective carrier temperatures. The solutions are discretized on a large grid, which typically comprises thousands to hundreds of thousands of nodes. In a sense, such a grid may be viewed as an extremely complicated electrical network. We should be able to extract workable equivalent circuit elements by a systematic reduction of the solution files — appropriately lumping together different nodes that are seen to be at the same potential, replacing streams of current by resistors, etc. Of course, this is precisely what a device physicist is doing implicitly while constructing an equivalent circuit based on a physical picture of the device. Our goal should be to automate this process, developing a robust procedure that would act as a postprocessor to device simulators — producing equivalent circuits of any desired complexity to any multi-terminal semiconductor structure under any operating conditions, that the device simulator itself can model.

In this approach, the relation between the physical picture provided by the simulator and that which exists in the real semiconductor structure is not to be challenged. Instead, we take the simulator model as *infallible* and investigate means for reducing that model to an equivalent circuit. Is this model reduction always possible? After all, the physical world in its complexity seems to go far beyond the effects that can be described by lumped-element electrical circuits. In the original program, as formulated by one of us [1], it was assumed that a circuit representation should always be possible so long as carrier concentrations and transport can be adequately described by carrier quasi Fermi levels (QFL)

and their gradients. This description naturally takes into account non-transport processes such as recombination, and hence describes currents flowing in real space and momentum space on equal footing. However, it was not clear initially how to include the effects of electrostatics (Poisson's equation) and the coexistence of conduction and displacement currents. A rigorous treatment due to Sah [2], based on previous work by Linvill [3], provided a circuit representation for both the Poisson and the transport equations. However, the original formulation was valid only in the limit of an infinitesimal semiconductor region. A breakthrough came with an integral derivation of circuit equations [4] which extended the model to regions of arbitrary size and enabled the methodology for automatic generation of circuits from the device simulation.

In this paper we review the essential elements of this methodology and discuss its potential and limitations. In Section 2 we introduce the technique using a simple electrostatic problem, including only ideal conductors, as an example. In Section 3 we generalize the picture to include charge transport in semiconductors. Section 4 is a review of past, current, and future work in a variety of application areas. In Section 5 we discuss fine points in the method implementation, and in Section 6 we comment on the advantages of the technique in comparison with black-box and table-based methods.

2 MODEL GENERATION METHODOLOGY

Our model extraction methodology is based on the calibration of a physically-based equivalent circuit by a numerical solution of the relevant equations. Let us consider for example an elementary electrostatic problem, comprising n conductors. The n^2 elements C^{kl} of the capacitance matrix can be computed from a solution of the Poisson equation, when a test voltage is applied to one of the terminals. The capacitance term C^{kl} is defined as[1]

$$C^{kl} = -\frac{\delta Q_k}{\delta V_l}, \tag{1}$$

where δV_l is the variation in voltage applied to conductor l, and δQ_k is the variation in the charge induced on conductor k.

The capacitance-matrix representation is rigorous, but requires a large number of coefficients. In circuit terms, each node is connected to $n-1$ other nodes via a capacitor, thus giving rise to $n(n-1)/2$ distinct circuit elements. It is well known that the capacitance matrix is sparse, i.e., a large number of elements is negligible due to screening. Taking advantage of this property, we can define a more compact representation, where each conductor is connected to a small set of nearest neighbors (Fig. 1). We denote the set of neighbors

[1] We use superscripts instead of the more common subscript notation, for consistency with symbols introduced later.

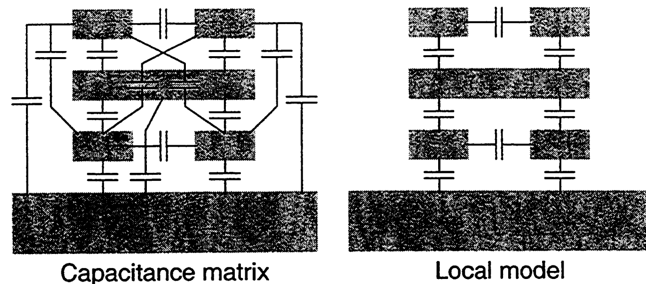

Figure 1: Left: Full capacitance matrix for five conductors over a ground plane. Right: Simplified local model.

of conductor k by $L^k = \{l^{k1}, l^{k2} \cdots l^{kn^k}\}$. For conductor k, we define a set of dielectric capacitances C_d^{kl}, from k to each of its neighbors in L^k. Applying a stimulus δV_k to conductor k, the effective capacitance element C_d^{kl} is defined as

$$C_d^{kl} = \frac{1}{\delta V^k} \int_{S^{kl}} dS \cdot \mathcal{E}, \tag{2}$$

where $\mathcal{E}$ is the electric field as obtained from the solution of the Poisson equation. The capacitance is now defined as the flux of the displacement vector from k to l, divided by the applied voltage stimulus. Even though this representation is not rigorous, it is has a clear physical interpretation, and it is more accurate than simply neglecting small terms in the capacitance matrix. In fact, it is simply shown from the Gauss theorem that

$$\sum_{l \in L^k} C_d^{kl} = \sum_{j \neq k} C^{kj} = -C^{kk}, \tag{3}$$

i.e., the small number of terms in the compact capacitance representation includes the effect of elements in the capacitance matrix not explicitly accounted for in the model.

From the above example, we can identify the main features of the model generation technique:

1. A simplified, but physically sound, circuit topology is employed to represent a complex system.
2. Expressions for the numerical values of the circuit elements are derived from integral equations. This ensures that basic conservation laws are obeyed in the resulting model.
3. Model calibration is obtained from a numerical solution of the microscopic equations, where one or more *stimuli* are applied to the system, and the resulting response is plugged into the integral equations which define element values.

In the example above, the topology is derived from simple geometric considerations, by neglecting coupling to distant conductors. The integral equation used to derive Eq. (2) is the Gauss theorem. The stimulus is the small-signal voltage applied to conductor k.

It is apparent that the simplified topology shown in Fig. 1 may not be a good model for the problem at hand. For example, the neglect of fringe capacitances between the first and third conductor levels could be disastrous if an accurate crosstalk estimation were needed. Moreover, there is some ambiguity in the definition of the dielectric capacitance in Eq. (2). In principle two different values for the capacitance connecting nodes k and l are obtained, one by applying a stimulus to conductor k, and a different one when the stimulus is applied to conductor l:

$$C_d^{lk} = \frac{1}{\delta V^l} \int_{S^{lk}} dS \cdot \mathcal{E}. \qquad (4)$$

Of course it is highly desirable to obtain a model including only reciprocal capacitors. Nevertheless, if the circuit topology is sound, then C_d^{kl} and C_d^{lk} will not be very different, and the error can be minimized by taking the average of the values obtained from the two stimuli. Generalizing the above considerations, we obtain the fourth feature of the method:

4. The accuracy of the model depends on a good choice of topology and stimuli.

One crucial feature of the integral-equation approach is that, if the conductors and the dielectric are partitioned into an infinite number of very small regions, the integral equations turn into differential equations, and the method becomes rigorous (after all, Poisson's equation is also a local microscopic model). Therefore, even though different choices of topologies and stimuli will yield various degrees of accuracy, the exact solution can always be achieved by increasing the model complexity.

3 SEMICONDUCTOR TRANSPORT MODEL

In the previous section, we only considered the Poisson equation, which models electrostatic interactions. The method can be extended to include also electron and hole transport, and generation/recombination mechanisms. The device, or simulation domain, is partitioned into discrete volumes. A circuit building block is associated with each volume Ω^k, with elements connecting it to its neighbors. The full equivalent-circuit block for two volumes Ω^k and Ω^l, and the surface S^{kl} between them, is shown in Fig. 2 [4]. The dielectric capacitor C_d^{kl} previously mentioned connects the electrostatic potentials V_i^k and V_i^l. Capacitors C_p^k and C_n^k model hole and electron charge storage, respectively, and connect the electrostatic potential node to the hole and electron quasi-Fermi levels V_p^k and V_n^k. Current sources I_p^{kl} and I_n^{kl} describe hole and electron current flowing between Ω^k and Ω^l. Finally, generation-recombination (G-R) is described to first order by a resistor R_r^k connecting the electron and hole QFLs V_n^k and V_p^k, so that the G-R rate depends on the energy difference between the two levels (i.e., the quantity $np - n_i^2$). External carrier generation (e.g., due to photon absorption) is likewise modeled by the current source I_g^k connecting nodes V_n^k and V_p^k.

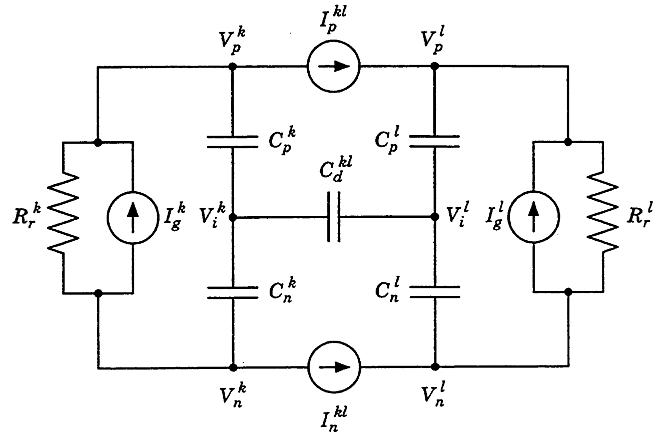

Figure 2: Circuit topology for two regions of semiconductor, labeled k and l, respectively, accounting for charge storage in each, and exchange of conduction and displacement currents between them. Generation and recombination elements are also shown.

All the currents and charges for the elements in the equivalent circuit in Fig. 2 are nonlinear functions of the applied voltages. Clearly, some elements will be more linear than others. For example, the dielectric capacitance is almost linear, due to the weak dependence of the depletion widths on the potential drops. On the other hand, the charge storage capacitors are highly nonlinear, due to the exponential dependence of the charge on the energy levels. In a circuit simulation, nonlinear elements will be represented by table-based interpolation schemes, where the data points (e.g., total electron charge Q_n^k as a function of the driving voltage $V_i^k - V_n^k$) are tabulated for a matrix of bias points. In a simplified implementation, a small-signal model for a single bias point can be obtained by linearizing all the elements.

The calibration of the semiconductor equivalent circuit must be obtained from a numerical solution of the Poisson equation and the continuity equations for electrons and holes. We obtain such solutions from the device simulator PADRE [5]. In order to obtain values for the equivalent-circuit elements, numerical integrations of the current, charges and electric fields are performed on the output of the device simulator. PADRE is based on the semiconductor transport equations, resulting from the first two moments of the Boltzmann kinetic equation. This includes the drift-diffusion equations and the carrier temperature transport equations for both kinds of carriers. All these can be incorporated *rigorously* in our methodology in the sense that the automatically derived circuit, *if fine enough,* will give results indistinguishable from those obtained by the device simulation.

How fine is fine enough? Experience with quasi one-one dimensional bipolar circuits [4] suggests that our procedure is robust and converges rapidly, using a number of elements

orders of magnitude smaller than the mesh points employed in PADRE. This is not surprising, since each of our circuit elements includes the knowledge of the full solution of the differential equations. The number of circuit elements we end up with is comparable to or less than that usually employed in "non-physical" fitting procedures. Naturally, the number of elements will expand for two- and three-dimensional simulations, but we can expect it to remain manageable. However, it should be understood that approximate circuits containing a relatively small number of elements may not be unique.

It should be also clearly understood that the rigor of our approach is closely linked to the fact that on the physical level we are dealing with the first two moments of the Boltzmann equation only, where the resultant differential equations admit of a simple circuit representation. Dealing with various nonlocal phenomena which cannot be reduced to first moments, physical device simulators must incorporate full Boltzmann solvers, such as Monte Carlo postprocessors. Needless to say, in this situation we are leaving the "rigorous" terrain in the attempt to construct an equivalent circuit. Nevertheless, in those cases when these nonlocal effects may be treated as pseudolocal (with modified transport parameters) the present approach should be expected to give a reasonable approximation, since circuit elements are calibrated on simulations which do include such effects. This empirical, but effective, recalibration is similar to the way velocity saturation is included in drift-diffusion models, not by including the electron temperature in the model, but simply introducing an artificial limitation of the velocity at high electric fields.

4 APPLICATIONS

4.1 Bipolar devices

The automatic model extraction technique has been initially applied to *pn* junctions and bipolar transistors. Bipolar devices are good testbeds for this approach, due to their one-dimensional nature which facilitates the extraction of data from the numerical simulation. At the same time, the correct prediction of the high-injection and high-frequency behavior even of the simplest *pn* junction is a nontrivial modeling problem, which has stimulated a substantial amount of work even in recent times [6], [7]. Fig. 3 shows results for the low-frequency behavior of a uniformly-doped *pn* junction. A three-section model was employed, with two blocks for the p and n quasi-neutral regions and one for the depletion region. The change of sign of the imaginary part of the admittance corresponding to a high-injection inductive effect, is correctly modeled. Note that this result was obtained from a completely automatic procedure, which autonomously divided the device into discrete regions, based on the location of the peaks of the differential charge concentration [8]. Also, the circuit sections were not specifically optimized for modeling quasi-neutral or depleted regions, but the program was able to find appropriate values of the circuit elements to perform the correct functionality. The same

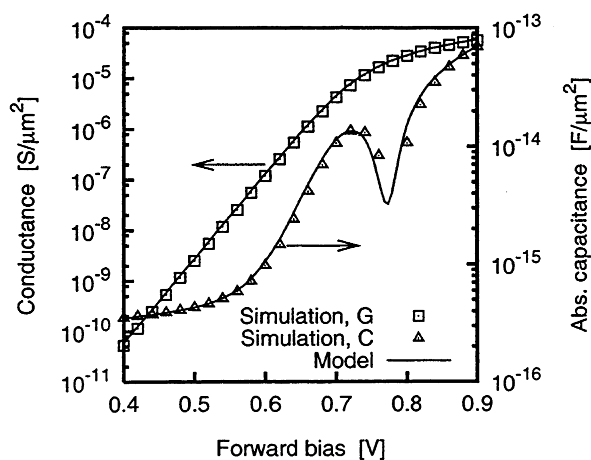

Figure 3: Small-signal conductance G and capacitance C at 100 kHz for a symmetric pn junction with $5\mu m$ *long p and n regions of doping* $10^{16}cm^{-3}$. *Symbols show device-simulation results. The dip in the capacitance corresponds to a change of sign at 0.77 V.*

identical procedure was applied to a $0.25\,\mu m$ bipolar transistor, yielding excellent match of the equivalent circuit to the ac device simulation up to the device cutoff frequency [4]. In this case, only five circuit sections were employed, three for the quasi-neutral regions (emitter, base, collector) and two for the base-emitter and base-collector depletion regions.

4.2 Optoelectronic devices

By introducing carrier generation and recombination, the BJT modeling procedure was extended to reproduce the transient behavior of a phototransistor. The base of the transistor was left open, while the optical signal was simulated by a uniform carrier generation. Figure 4 shows the small-signal transient collector current in response to a small step in light intensity. Note that since a linear extraction was performed, the step amplitude was maintained small enough not to cause significant nonlinear effects. The two-step response is correctly reproduced by the compact model, including the delayed response of the transistor due to base-emitter charge storage. Also in this case, the extraction was completely automatic. Since the optical response was desired, an optical stimulus was employed. The element values were defined from the small-signal response to a small variation in light intensity.

4.3 Device parasitics

In the preceding two sections we have shown examples of the validation of our model generation technique on traditional devices, for which successful compact models already exist. However, there is a wide range of parasitic effects which are not adequately covered by existing models, and whose dependence on the technological parameters

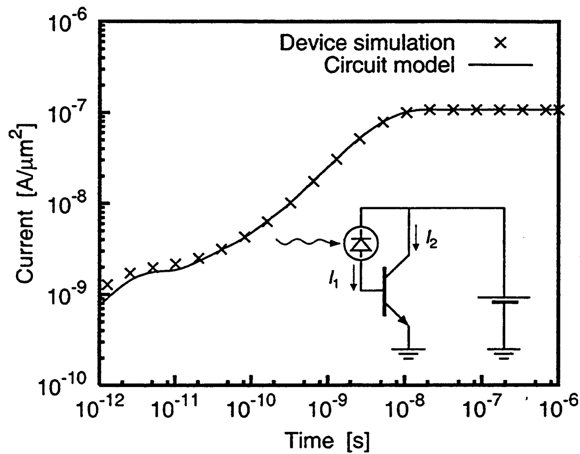

Figure 4: Time transient of output current for a simple phototransistor, for a step increase of light intensity. Numerical device simulation (symbols) is compared to equivalent circuit (solid line). The inset shows the schematics of device operation. The initial small increase of current (in the picosecond range) is due to the arrival of primary photocurrent I_1 to the collector, while the second step (reaching saturation at about 10^{-8} s) is due to the current $I_2 = \beta I_1$ by transistor action.

requires new models to be developed almost continuously. Examples include MOSFET substrate coupling, distributed *RC* effects in isolation wells, substrate capacitive currents and eddy currents in spiral inductors, etc. Such problems do not present great obstacles from the point of view of circuit topology and model extraction, although the intrinsically three-dimensional geometries require a considerable effort in partitioning the device (see Section 5 below).

4.4 Interconnections

Interconnection networks represent a challenge for traditional modeling techniques, and an opportunity for employing new approaches. The accurate modeling of capacitive, resistive, and inductive parasitic elements is key to effective IC design [9]. Such elements involve complex electromagnetics (e.g., skin effect), and must be extracted for a variety of possible layouts. A modular approach to parasitic extraction offers the following advantages:

1. The extraction does not depend on analytical expressions, which have been found to be short-lived due to the impetuous technological progress.
2. Unlike physical models (e.g., fast solvers), an equivalent-circuit-based model lends itself to postprocessing such as model reduction, interpolation, and transformation into symbolic form suitable for synthesis and optimization.
3. Large-scale interconnection networks can be divided into smaller networks and models can be separately extracted and merged. Again, this is a major advantage over physical solvers, allowing application to full-chip interconnect analysis which would otherwise require staggering computer resources.

While for capacitive and resistive parasitics a simplified version of the semiconductor-device building block of Fig. 2 can be employed (using only one type of charge carrier), inductive effects require an extension of the model. Specifically, we can include magnetostatic effects by adding a circuit branch corresponding to an integral equation for the magnetic field, by analogy with electrostatic interactions. The approach is in some ways similar to the partial-element equivalent circuit (PEEC) where a matrix of integral equations is interpreted as a set of circuit equations [10]. However, the present technique, based on intrinsically local models, is ideally suited for inductive effects, where matrix sparsification is a key issue. Moreover, in the PEEC approach, as in Sah's original method, element values are computed from analytical expressions, while in our methodology they are extracted from a solutions of the physical equations. This property promises a better accuracy with a smaller number of circuit elements.

4.5 Self-heating and thermal coupling

The same considerations made above for interconnects also apply to thermal effects in integrated circuits. High-performance technological solutions such as low-K dielectrics, SOI substrates, deep-trench isolation, and three-dimensional integration all contribute to a degradation of heat removal. The consequent temperature gradients can have a dramatic impact on the performance of analog and digital circuits, and on electromigration [11]–[13]. The model-generation methodology can be easily adapted to deal with thermal elements, so that, for example, thermal capacitance can be obtained as an incremental ratio of thermal energy to temperature, and thermal resistance as a ratio of temperature increase to differential heat flow. A "thermal network" is then defined, composed of material regions which exchange heat through the interfaces between them. Each region k has a capacitance C_{th}^k to ground which represents its thermal energy, while each interface S^{kl} is associated to a thermal resistance R_{th}^{kl} which corresponds to the heat exchanged through it (Fig. 5). The dissipated power P_{diss}^k is represented by a current source charging the thermal capacitance. Note how the Kirchhoff current law for each temperature node corresponds to the first principle of thermodynamics (power in equals power out minus stored energy). This physically sound approach is likely to be more robust than empirical connections of thermal resistances and capacitances (e.g., a series connection of *RC* parallels [12]), which do have any meaningful interpretation. A typical device model will include a small number of regions, orders of magnitude less than in a typical simulation mesh. At the

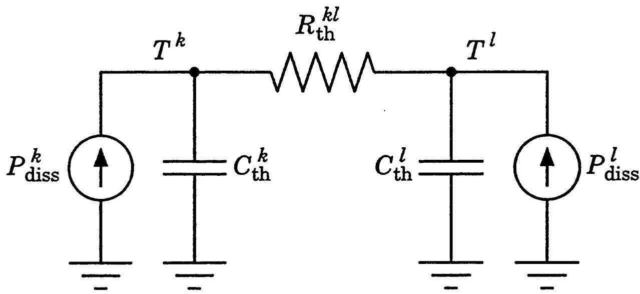

Figure 5: Circuit topology for two regions of semiconductor, labeled k and l, respectively, modeling thermal effects. The thermal capacitance C_{th}^k represents the storage of thermal energy, and is charged by the dissipated power P_{diss}^k. The thermal resistance R_{th}^{kl} models heat exchange between regions k and l.

same time, each element models the behavior of the corresponding volume or interface with great accuracy. This is due to the fact that the numerical values of thermal capacitances and resistances are not *guessed* from finite-difference approximations [14], but rather *computed* from the device simulation result. Thermal effects represent a significant gap in the state of the art of integrated circuit modeling, which is ideally filled by an efficient, technology-independent technique.

4.6 Hot-carrier and quantum-mechanical effects

So far we have assumed that charge storage can be adequately described by a single quasi-Fermi level. In many cases, the carrier population is not at thermal equilibrium, therefore more variables are needed to effectively describe its state. The thermal circuit described in the previous section can be extended to include the electron and hole effective temperatures. Circuit elements can model energy exchange between the lattice and the free carrier population, as a current flow between temperature nodes. This approach has the advantage of leaving the topology of the electrical circuit almost unchanged, and augmenting the thermal circuit with additional thermal capacitors. Another advantage of this approach is that it parallels the methodology used in modeling hot carrier effects in PADRE [5] by incorporating energy transport equations into the PDE system to be solved. Using this approach we modeled the real-space transfer in the charge-injection transistor (CHINT) [15], [16], which is a device essentially based on hot electron effects. Subtle and unusual effects, both static (including multiply connected IV characteristic) and dynamic (hot-electron domain formation) were successfully simulated and understood and yet we were unable to derive a viable physically-based circuit model for the device.[2]

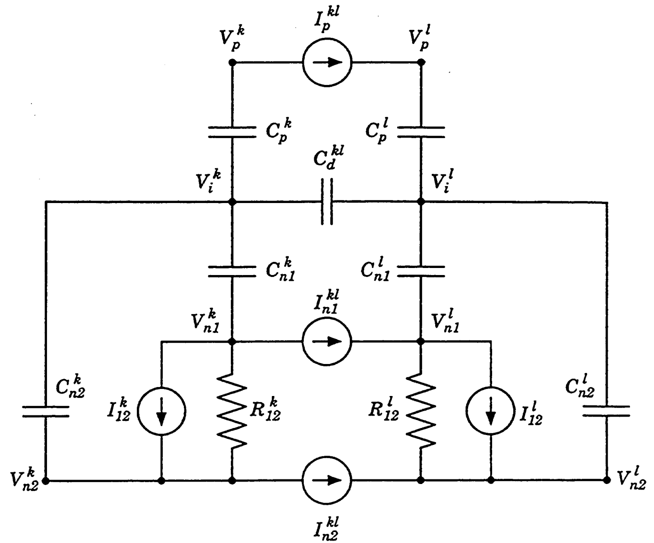

Figure 6: Extension of the equivalent circuit of Fig. 2 to account for two electron populations, described by quasi-Fermi levels V_{n1} and V_{n2}. The two populations may correspond to two subbands in a quantized electron gas, or to 'cold' and 'hot' carriers in a high-field region.

An alternate way of modeling the same effect is by the use of multiple quasi-Fermi levels, each describing a separate carrier population. For example, the occupancy of low- and high-energy states can be modeled by separate QFLs for the 'cold' and 'hot' carriers (Fig. 6). A thermalizing resistor R_{12}^k would tend to equalize the two levels, while a current source I_{12}^k would transfer charge from the 'cold' to the 'hot' populations, due to the heating action of the electric field. This topology (which is similar to the one originally adopted by Sah to describe MOS interface traps [17]) is rather crude if the carrier distribution is indeed a heated Maxwellian, as it happens at moderate electric fields. However, in this approach a separate thermal subcircuit is not needed, making the model more compact. Moreover, the topology can be generalized to account for more energy levels, allowing the modeling of phenomena with multiple thresholds, such as impact ionization and oxide injection.

The same multiple-QFL approach can be employed to represent a multiple-subband structure in a two-dimensional electron gas (2DEG). A separate Fermi level would be defined for each subband, adding one or more extra 'rails' to the circuit of Fig. 2. In this case, the thermalizing resistor R_{12}^k represents intersubband scattering.

[2]The CHINT is a three-terminal device based on the real-space transfer of hot electrons between independently contacted semiconductor layers. The voltage applied to the third CHINT terminal controls the negative differential resistance between the two other terminals. This property is attractive, for example, for the implementation of voltage-controlled oscillators. Circuit design using charge-transfer devices has been hampered, however, by the absence of a workable equivalent RF circuit of the CHINT. The frustration felt by one of us (SL) due to this state of affairs was in fact an important impetus for initiating the current program.

5 IMPLEMENTATION ISSUES

As outlined in the preceding sections, there is a number of theoretical and practical issues which must be addressed in the implementation of the model generation technique. Even though in the limit of an infinite number of elements the model is rigorous, it is obvious that a satisfactory accuracy must be obtained using the smallest possible number of elements. In turn, a low complexity can be achieved by adopting a good circuit topology, a good partitioning of the device, and a good set of stimuli.

Choice of circuit topology is the most important step in the procedure. In principle, the topology and type of elements is arbitrary. For example, electron current flow can be modeled by a simple resistor connecting two electron QFLs. This representation is satisfactory for simple majority transport, but may not be well suited to diffusion, where the current is mainly controlled by the electron concentration at the injecting end of the device. More importantly, and less obviously, a resistor is defined by only one numerical value, i.e., there is only one degree of freedom in fitting numerical simulations. In many cases, one needs to simultaneously satisfy two or more constraints, for example, the forward transconductance and the Early effect in a bipolar transistor. The availability of two or more parameters increases the representational power of the model. In the example above, the simple resistor can be replaced by a parallel of a resistor and a voltage-controlled current source, where the controlling voltage may be the difference between the electron QFL and the electrostatic potential, which is directly related to the electron concentration [4].

In special circumstances, several completely different topologies exists to represent a given physical effect. One example is the hot-carrier equivalent circuit described in Section 4.6. The choice of model is dictated by the particular application, and may require some empirical iterations.

The task of partitioning a device into discrete domains is also challenging. In one dimension, partitioning consists in identifying a set of points which separate one region from its neighbors. In 2D and 3D, device partitioning becomes a serious problem in computational geometry. Drastic simplifications can be performed for the case of simple geometries such as interconnections with constant cross-section, so that regions can be separated by horizontal and vertical planes. However, the general case of 3D devices with curved boundaries (e.g., source/drain depletion regions) needs substantial work. Fortunately, effective meshing algorithms are an essential part of most modern simulation codes. Once again we can rely on a state-of-the-art modeling program, and obtain a partitioning by aggregating mesh nodes based on topological and physical criteria.

Finally, the choice of stimuli is crucial to the success of the model extraction process. In general, one would like to have enough stimuli to properly calibrate all element values, but not so many that the calibration problem is overconstrained. Satisfying a large number of conditions requires a large number of parameters, which leads to complicated circuit elements such as nonreciprocal capacitance and inductance matrices. Such elements may be undesirable, mainly because they are hard to understand and can have unpredictable effects on circuit performance. On the other hand, the role of simple elements such as resistors and capacitors is easily understood, which allows feedback from the users of the model (circuit designers) to the device designers.

So far, we have considered only the case of model extraction from a full physical simulation, where external variables such as voltages and currents are applied to the entire structure. This procedure is optimal for active devices, where the simulation domain and number of terminals are both small. In the case of interconnection networks at the subcircuit or die level, the large number of terminals and the sheer size of the structure may make the method inapplicable to realistic cases. However, the technique can be extended to use 'synthetic' stimuli, where only a very simplified physical problem is solved, for example, by injecting voltages or currents directly into the region where the element extraction is being performed. This approach is being currently investigated and promises to boost performance significantly.

6 DISCUSSION

In this paper we presented a rather general methodology aimed at the derivation of equivalent lumped-element circuits from physical device simulation. The fact that our technique is riding on the back of physical modeling and does not work independently, is not its weakness but a major strength. It enables us to faithfully mimic the rigorous fine-mesh simulation with a relatively small number of elements. However, as discussed above, small circuits carry a price — they are not unique, and not all possible alternative implementation reach the same level of accuracy.

To assess the practical impact of this work, it is essential to compare the present approach to black-box and table-lookup techniques for compact model generation, which in various forms are used today, especially in the computer-aided design of microwave circuits. Typically, each of such methods is located at some point in an ideal plane of generality versus accuracy. At one end, we have the true black-box models, where generic fitting functions such as polynomials or splines are used to model the behavior of an unknown device [18]. Clearly, in order to achieve satisfactory accuracy in a variety of applications, such models require a large number of coefficients. At the other end of the spectrum, we find table-based equivalent circuits, where some or all the elements of a predefined circuit topology have values which are obtained from a table lookup [19]–[22]. If the topology is applicable to the device under study, such models achieve high accuracy, and their calibration is efficient due to the small number of model parameters. Due to the adoption of a fixed topology, table-based models suffer from the same lack of generality, and technology dependence, of the more traditional compact modeling techniques. The mod-

els presented in this paper are closer to the latter class than to black-box models. However, since a different topology is automatically generated for each device, the range of application is vastly extended. In this respect, purely from the point of view of taxonomy, one could speak of *adaptive-topology table-lookup models.*

Finally, as illustrated in Sec. 4, the mathematical formalism presented here extends beyond the modeling of transistors, and offers a unified description of electrical, magnetic, thermal, and nonequilibrium effects in integrated circuits. New physical effects can be included by the addition of new integral equations and/or new simulation codes into the model-generation flow. Since the resulting circuit is physically based, secondary effects such as noise and temperature dependence can be added in a consistent manner, rather than empirically. The larger computational effort required by the model-generation technique is largely outweighed by the reduction in human labor, development time, and errors.

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