

Comprehensive Modeling of MOS Transistors in a 0.35um Technology for Analog and Digital Applications

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ABSTRACT

The purpose of this work is to present a comprehensive report of the MOS transistor characteristics in a 0.35um technology, both types being surface devices. Results include extensive geometrical and temperature dependencies of the most important transistor parameters needed for all applications specially the Analog. N and PMOS threshold voltage, saturation current, maximum transconductance, as well as the output resistance in saturation and linear region were the selected parameters for this investigation. Graphical results show accurate dependency of each of these parameters on geometry and temperature.

Keywords: MOS Modeling, 0.35um MOS Transistor, Temperature Effects in MOS Transistors.

1 INTRODUCTION

MOS transistor with a nominal channel length of 0.35 um has been used in semiconductor technology for less than a decade now. The development and utilization of generations of MOS transistors have happened at a fast pace, one after another. Papers from the pioneering developers of the 0.35um MOS were seen in late 80's and early 90's [1,2]. In the development phase, as is always the case, some characteristics of the new device were published. Subsequently the 0.35um transistor entered the line of production. Since then, how much information pertaining to the actual 0.35um transistor as manufactured has been published? How many of the older assumptions, and specific features pertaining to the older MOS generations are still valid? This paper is an attempt to answer some these questions and shed light on some of the most commonly needed and useful characteristics of the 0.35 um transistor. All the presented information is backed up by silicon from the 0.35um line of production.

In this work, a group of parameters that were considered important in terms of characterization of any MOS transistor were selected. These included the threshold voltage (V_t), saturation current (I_{dsat}), maximum transconductance (G_m), output resistance in saturation region (R_o), and output resistance in linear region (R_{Lin}). The inclusion of resistances and G_m are specially important for analog applications. The goal of this paper is to report a detailed characterization of each of these parameters in the form of their dependencies on geometry and temperature. Both N and PMOS transistors are included.

2 METHODOLOGY

The first step of this work was to develop a reliable model for the MOS transistors of each type (N and P) that could be extensively use it to investigate the transistor behavior in all operating regions. While plenty of devices were available on silicon to be used for any characterization purposes, still an accurate model is more flexible, easier to use and faster to work with. Needless to say, the accuracy of the model is the key point.

The selected model for this purpose was Philips MOS Model 9 (MM9). The model has been used in industry since 1995 [3] and has been accepted as the company wide spice model in STMicroelectronics. So, the approach was to use the available silicon from the 0.35 um technology, do an extensive data collection, and build reliable MM9 models as the first step. Then use the model to extract the information of interest, that is the device parameters of interest for a variety of geometries and temperatures. And finally, summarize the results in graphical and tabulated forms.

The MOS transistors used for data collection were available on modeling and characterization scribes included on each wafer on 0.35um technology line. These provided a range of N and PMOS transistors with different geometries. Ten geometries of each device were available and used for extensive data collection and MM9 model generation. A temperature range of 0C to 125C was used for the extraction of temperature coefficients used in MM9. Detailed description of the modeling work is not the purpose of this work. Accurate matches between the data and the models were obtained. Table 1 provides a brief comparison of silicon vs. model predictions. Additionally, ring oscillators with a variety of geometries were measured and simulated as a further check of accuracy for the models. Simulated and measured propagation delays agreed with better than 3% of accuracy.

The MM9 models for N and PMOS devices were then accepted and considered as accurate mathematical models for the transistors. They were also fine tuned to the nominal target values of the process. The nominal models were then used to generate the necessary device characteristics to extract the parameters of interest including V_t , I_{dsat} , G_m , R_o , and R_{Lin} (defined above). Eldo was used as the main simulation tool. These parameters were then extracted for thirty geometries and fourteen temperatures. The selection of such a wide range of transistor length and width values covers any possible geometry used in design. Results were summarized and are presented here. They provide an

accurate view of the transistors main parameters and their dependencies on geometry and temperature.

3 RESULTS AND DISCUSSION

Results are presented through a number of figures. At the same time, Table 1 summarizes the results of temperature dependence of the calculated parameters. The observed roll-on voltages (reverse short channel effect) for the N and PMOS devices are 23 and 8 mV respectively. While the threshold voltages show a temperature coefficient of ~ -1.0 mV/C, the roll-on voltage is almost independent of temperature. Figure 1 shows the threshold voltage characteristics for both N and PMOS transistors in graphical form. Channel lengths from 0.3 μ m to 10 μ m are covered. The temperature range for these results is 5 to 125C.

The saturation current (I_{dsat}) is the device current at $V_{gsr}=V_{ds}=3.3V$ (since this is a 3.3V process). Figure 2 shows linear variation of I_{dsat} vs. the inverse of the drawn length for the PMOS, but nonlinear for the NMOS. The reason for this difference should be sought in saturation velocity issues for the two device types. The saturation velocities (V_{sat}) for electrons and holes are close and on the order of $\sim 1E10$ cm/s according to different models discussed best by Selberherr [4]. The mobility, however, is higher by about 3x for electrons compared to holes. So, for the same applied voltage and comparable internal electric fields, electrons will experience higher velocities and are more prone to reaching V_{sat} showing nonlinear I_{dsat} curves. But holes are drifting below saturation velocity having linear I_{dsat} curves.

Also, according to Table 1 the average rate of change of I_{dsat} with temperature is almost proportional to the magnitude of the current for that device. But the temperature dependency of this parameter is not linear for any of the device types. This is mostly because of the exponential decay of the mobility parameter for electrons and holes as a function of temperature.

Figures 3, 4, and 5 show the variations of G_m vs. $1/L$, R_o , and R_{Lin} as a function of L . All results show the temperature effects too. After Figure 1, fewer temperatures are shown on each graph for more readable results. For G_m a negative temperature coefficient with nonlinear dependency on temperature is seen. This is expected due to the direct relation of the transconductance to the carrier mobility. The saturation region output resistance characteristics, R_o vs. drawn length L , clearly have both linear and nonlinear regions. The linear region for NMOS starts at lengths as large as 5 μ m. For the PMOS this number is close to 3 μ m. Below these values, the length dependency of R_o is heavily nonlinear. Device phenomena affecting the saturation region of the MOS transistor, including channel length modulation, drain barrier lowering effect, etc. are determining the shape of these curves. These phenomena become dominant and serious at lower values of L hence contributing to the nonlinear portion. At higher values of

L , however, the simple theory of MOS is acceptable where R_o shows linear dependence on L . Information in figure 4 is valuable for designs using the MOS as a highly resistive load. A positive temperature coefficient with close-to-linear temperature dependency is observed.

The MOS output resistance in the linear region, R_{Lin} , on the other hand, shows a complete linear dependency on drawn length. It has a positive temperature coefficient for each device type and the temperature dependency is almost linear. Information presented in Figure 5 is valuable for designs utilizing the MOS transistor as a voltage controlled resistor operating in the linear portion of the output characteristics. Table 1 shows the extracted temperature coefficients for each of these parameters.

The effects of device width (W) on device characteristics are also partially presented. The output resistance dependence on $1/W$ is linear as expected. As the width is reduced, below a certain limit deviation from linearity is expected. For both devices, the accuracy of the model at very narrow width values (less than 0.7 μ m) is questionable too. Figure 6 shows the graphical dependence of R_{Lin} on $1/W$. This covers only the reliable portion of the results.

4 Summary and Conclusions

Accurate MM9 models for N and PMOS devices were made based on data from silicon. Extensive temperature data in the range of 0 to 125C were used for the extraction of temperature coefficients in the models. The models were then used to simulate MOS performance under different operating conditions for the extraction of five major parameters. Tabulated and graphical results show detailed variations of the selected parameters. Reverse short channel effect is as high as 23mV for NMOS and 8mV for the PMOS, and the values almost independent of temperature. The output resistance in saturation region (R_o) shows linear dependence on L at values higher than 5 μ m for NMOS and 3 μ m for PMOS. Below these values of L , the curves are nonlinear due to complicated short channel effects discussed. The physical bases for the different figures are discussed too.

References

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Parameter	Measured or Simulated	T = 25° C		T = 75° C		T = 125° C		Rate of Change with T	
		NMOS	PMOS	NMOS	PMOS	NMOS	PMOS	NMOS	PMOS
VT (V)	S	0.542	-0.557	0.491	-0.506	0.445	-0.456	-9.69E-04	1.01E-03
	M	0.547	-0.568	0.499	-0.518	0.450	-0.467	-9.68E-04	1.01E-03
VT Roll-on (V)	S	0.023	0.008	0.025	0.008	0.026	0.007	3.41E-05	-8.60E-06
	M	0.024	0.008	0.026	0.008	0.027	0.007	3.40E-05	-8.61E-06
IDSAT (A)	S	5.47E-03	2.49E-03	4.94E-03	2.31E-03	4.67E-03	2.16E-03	-7.93E-06	-3.25E-06
	M	5.44E-03	2.44E-03	5.04E-03	2.28E-03	4.66E-03	2.11E-03	-7.82E-06	-3.23E-06
GM (A/V)	S	2.12E-04	5.72E-05	1.67E-04	4.79E-05	1.37E-04	4.13E-05	-7.54E-07	-1.59E-07
	M	2.11E-04	5.60E-05	1.74E-04	4.81E-05	1.36E-04	4.02E-05	-7.54E-07	-1.58E-07
Ro (Ohms)	S	1.15E+04	7.20E+03	1.25E+04	7.49E+03	1.28E+04	7.89E+03	1.34E+01	6.95E+00
	M	1.16E+04	7.27E+03	1.23E+04	7.62E+03	1.30E+04	7.96E+03	1.35E+01	6.96E+00
RLin (Ohms)	S	1.64E+02	5.52E+02	1.93E+02	6.12E+02	2.16E+02	6.59E+02	5.21E-01	1.08E+00
	M	1.65E+02	5.63E+02	1.92E+02	6.17E+02	2.18E+02	6.72E+02	5.26E-01	1.09E+00

Table 1. A brief comparison of the measured data and simulation results for N and PMOS 10x0.35um devices at three temperatures.



