The Landauer Approach to the Critical Source-Channel Barrier in MOSFETs

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ABSTRACT

A simple treatment of the nano-scale MOSFET in the spirit of the Landauer approach to transport in mesoscopic structures is described. First, the essential physics is illustrated by examining numerical simulations. Next, the analytical theory of the ballistic MOSFET is discussed, and finally, the role of scattering in nano-scale MOSFETs is discussed.

Keywords: MOSFET, transistor, ballistic transport, nanoelectronics.

1 INTRODUCTION

Silicon MOSFET channel lengths are rapidly approaching 10nm where traditional modeling approaches lose validity. Our objective is to describe an alternative approach to MOSFET models based on concepts that have been widely used in mesoscopic physics [1]. Figure 1 illustrates the basic physical picture; it shows the lowest conduction subband energy vs. position under high gate and drain bias. The height of the source-channel barrier is modulated by the gate voltage. The drain current increases as the barrier height in reduced by the increasing gate voltage. A MOSFET is similar to a bipolar transistor, except that in a bipolar transistor the barrier height is directly modulated by the emitter-base voltage while in the MOSFET it is modulated indirectly by the gate voltage [2]. Our objective is to discuss a theory of the nano-MOSFET based on this physical picture.

2 PHYSICS OF NANO-MOSFETS

MOSFETs are complicated by 2D electrostatics and strong, off-equilibrium transport in the presence of rapidly varying electric fields. These effects have been recently examined by 2D, numerical simulations using the non-equilibrium Green's function approach [3, 4] (see also, [5] for an earlier quantum scale study of 10 nm MOSFETs). For extremely short channel lengths, quantum mechanical tunneling from source to drain (through the barrier) degrades device performance, but for channel lengths above 10 nm, MOSFETs behave classically. We will, therefore, adopt a classical model in this talk. Scattering complicates the analysis, but some key elements of the essential physics can be established by numerical simulations of ballistic MOSFETs. Figure 2, for example, shows the numerically computed carrier distribution vs. position for a 10nm channel length ballistic MOSFET operating under high-bias [6]. The carrier distribution function is seen to be strongly distorted from its equilibrium value. Note, for example, the ballistic peak within the channel.

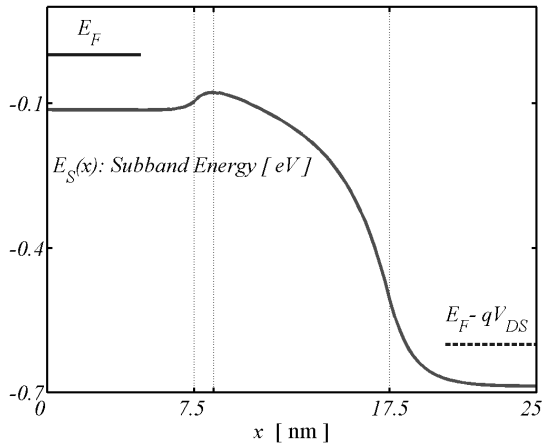

Figure 1: Conduction subband energy vs. position for a MOSFET under high gate and drain bias.

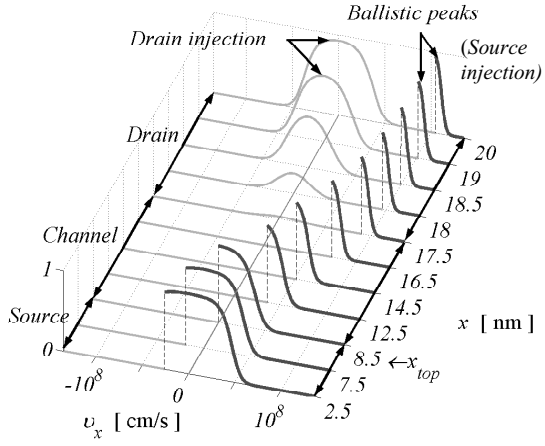

Figure 2: Electron distribution function vs. position for a ballistic n-MOSFET as computed under high gate and drain bias [6].

The complex shape of the carrier distribution function would seem to preclude simple, analytical modeling, but Fig. 3 shows that things are much simpler at the top of the source-channel barrier. This figure shows the carrier distribution function under high gate bias at four different drain voltages. For V_{DS} = 0, the distribution has an equilibrium shape; the positive half of the thermal distribution was injected from the thermal reservoir at the source and the negative half from the drain. As V_{DS} increases, the negative portion of the distribution diminishes. Note, however, that the positive half grows. This occurs because of the MOSFET's electrostatics. In an electrostatically well-designed MOSFET, the gate holds the charge at the top of the barrier approximately constant with drain bias. Above threshold, the value is $\approx C_G(V_{GS}-V_T)$, except for a shift of the threshold voltage, V_T, depending on the magnitude of the 2D short channel effects.

The key concepts illustrated by the numerical simulation are summarized as follows. First, the carrier distribution function at the top of the source-channel barrier consists of two thermal equilibrium halves, one injected from the source and the other from the drain. Second, as the drain bias increases, the negative portion of the distribution diminishes in size, but for an electrostatically well-designed MOSFET, the total carrier density at the top of the barrier is maintained at an approximately constant value. Finally, since the high V_{DS} distribution approaches a hemi-Fermi-Dirac distribution, the average velocity at the top of the barrier saturates at a limiting value, which is the average velocity of a thermal equilibrium Fermi-Dirac distribution. As discussed next, these key concepts can be used to develop an analytical theory of the ballistic MOSFET.

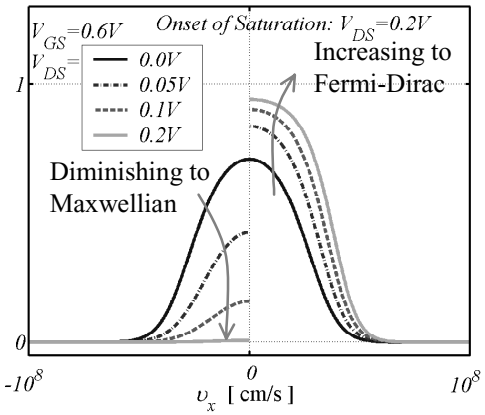

Figure 3: Electron distribution function at the top of the barrier as computed for four different drain bias [6].

3 THEORY OF THE BALLISTIC MOSFET

Figure 4 sketches the E-k relation at the top of the source-channel barrier. The positive k-states are populated by injection from the source according to the source Fermi level, E_F, and the negative k-states are populated from the drain according to the drain Fermi level, $E_F - qV_{DS}$. By assuming 2D statistics for the quantum confined carrier in the channel, we can relate the carrier populations in the positive and negative halves to their respective Fermi levels. Above threshold, MOS electrostatics then demands that the total carrier density is approximately independent of drain voltage, so we find

$$C_G(V_{GS}-V_T)\approx n_S^+(E_F)+n_S^-(E_F-qV_{DS})\,. \qquad (1)$$

Equation (1) is an equation for the location of the Fermi level. For a given device design, the gate capacitance, C_G, and threshold voltage, V_T, are determined. Equation (1) then determines the location of the Fermi level as a function of gate and drain bias. As the drain bias increases, n_S^- decreases, so E_F increases to maintain charge balance. This occurs physically by the gate electrostatically pushing down the source-channel barrier to let more electrons in from the source.

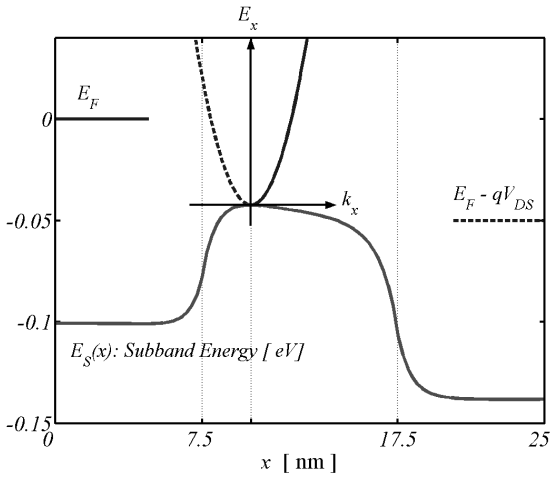

Figure 4: E-k relation at the top of the source-channel barrier showing the source and drain Fermi levels, E_F and $E_F - qV_{DS}$.

Having determined the Fermi level, the positive and negative fluxes can be evaluated by integrating over the populated states to obtain the drain current as

$$I_D = \Gamma^+(E_F) - \Gamma^-(E_F - qV_{DS})\,. \qquad (2)$$

The approach outlined here is essentially Natori's theory of the ballistic MOSFET, [7,8] which has been further developed by our group [9-11].

Using the approach outlined above, the I_{DS}-V_{DS} characteristic of a ballistic MOSFET is readily evaluated. The simple expressions for the on-current are illuminating. The on-current is the product of the charge density and the average velocity of an equilibrium hemi-Fermi–Dirac distribution. For non-degenerate conditions, we find

$$I_D = W\, C_G\left(V_{DD} - V_T\right)\left[\sqrt{2k_BT/\pi m^*}\right], \quad (3a)$$

which shows that the ballistic MOSFET's on-current is proportional to ($V_{GS} - V_T$), just as it is for a velocity saturated MOSFET. The channel velocity does saturate in a ballistic MOSFET, but it is the velocity at the top of the barrier that saturates, not the velocity near the drain. In practice, however, nondegenerate statistics do not apply above threshold. In the fully degenerate limit, Eq. (3) becomes

$$I_D = W\, C_G\left(V_{DD} - V_T\right)\left[\left(8\hbar/3m^*\right)\sqrt{C_G(V_{GS} - V_T)/q\pi}\right]. \quad (3b)$$

MOSFETs typically operate between these two limits, so $I_D \propto \left(V_{GS} - V_T\right)^{\alpha}$ where $1 < \alpha < 1.5$, which is very similar to the result obtained by traditional MOSFET models.

The linear region of the ballistic MOSFET is also of interest. For small V_{DS}, the drain current is

$$I_D = G_{CH} V_{DS}, \quad (4)$$

that is, a ballistic MOSFET shows a finite channel conductance. The expression for G_{CH} involves Fermi-Dirac integrals [10], but at $T = 0$, it reduces to

$$G_{CH} = M\left(2q^2/h\right), \quad (5)$$

the expected conductance of a ballistic conductor [1]. In Eq. (6), M is the number of occupied modes, which is proportional to the width, W, of the MOSFET.

4 CARRIER SCATTERING IN NANO-MOSFETS

In practice, MOSFETs are observed to deliver an on-current that is roughly 50% of the ballistic limit due to carrier backscattering [12, 13]. In the presence of scattering, the on-current can be expressed in terms of a channel transmission coefficient, T [14]. (A more involved expression for the complete I-V characteristic in terms of T can also be developed [15].) For the on-current, we assume, as for the ballistic MOSFET, that a current, I^+ is injected into the channel from the top of the barrier. Since only a fraction, T, of the injected current exits from the drain,

$$I_D = T\, I^+ \quad (6)$$

The carrier density at the top of the barrier consists of contributions from the positive and negative k-states. Because the large drain voltage cuts off injection from the drain, the negative k-states are populated by backscattering of the positive stream. As a result, the carrier density at the top of the barrier is

$$n_S(0) = \frac{I^+}{qW\upsilon^+} + \frac{(1-T)I^+}{qW\upsilon^-}. \quad (7)$$

If we assume that $\upsilon^+ \approx \upsilon^- \approx \tilde{\upsilon}_T$, then eq. (7) can be solved for I^+ and inserted in (6) to find

$$I_D = WC_G\left(V_{GS} - V_T\right)\left[\frac{T}{2-T}\right]\tilde{\upsilon}_T. \quad (8)$$

Under non-degenerate conditions, $\tilde{\upsilon}_T = \sqrt{2k_BT/\pi m^*}$, while in the degenerate limit, $\tilde{\upsilon}_T = \left(8\hbar/3m^*\right)\sqrt{C_G\left(V_{GS} - V_T\right)/q\pi}$. In the ballistic limit, $T = 1$, and Eq. (8) reduces to Eqs. (3). For typical MOSFETs, $T \approx 0.6$, so the on-current is 40-50% of the ballistic limit.

Understanding a nanoscale MOSFET boils down to understanding how the channel transmission coefficient depends on device structure, temperature, and bias. Under low VDS, the channel transmission coefficient is just the transmission coefficient for a field-free slab of length, L [1]

$$T = \frac{\lambda}{\lambda + L}, \quad (9)$$

where λ is the mean-free-path for backscatteirng. Typically, $T < 0.1$ for low V_{DS}, but for high VDS it increases to ≈ 0.4.

Computing T under high drain bias is complicated by the strong off-equilibrium transport effects that occur. It has, however, been argued that Eq. (9) can be applied to high bias condition if the channel length, L, is replaced by an effective length, ℓ, so that Eq. (9) becomes [14]

$$T = \frac{\lambda}{\lambda + \ell}. \quad (10)$$

Because ℓ is typically a small fraction of the channel length, scattering near the source is what controls the on-current.

A rigorous derivation of the high drain bias T is complicated by the strong off—equilibrium transport effects that occur in short channel devices. A simple argument, however, explains why the on-current is most sensitive to backscattering near the source. Consider Fig. 5, which shows an electron with energy, E, and kinetic energy, E_0, injected into the channel. It is important to note that Fig. 5 is a plot of the longitudinal energy, but an electron may backscatter at an angle (i.e. into a transverse mode). Only a fraction of the carrier that backscatter have sufficient longitudinal kinetic energy to return to the source, the others will be reflected by the channel potential and exit

the drain. The fraction that backscatter with sufficient longitudinal energy to return to the source is a decreasing function of distance into the channel [14], so scattering near the source is what controls the on-current.

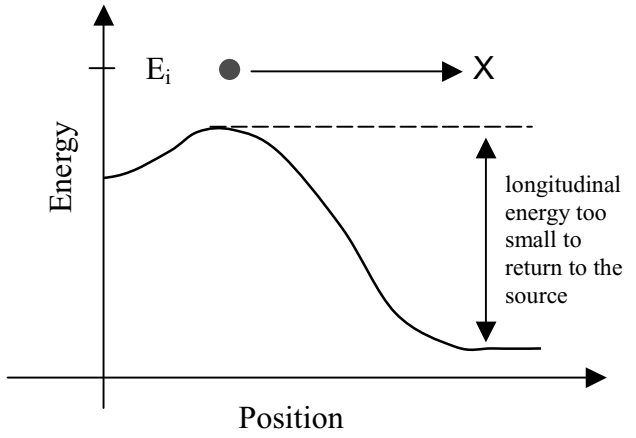

Figure 5: Illustration of an electron injected into the channel with energy, E_i. It backscatters at location, X, but only those with longitudinal energy above the dashed line can return to the source.

5 SUMMARY

We have outlined a simple theory that describes the essential features of nano-scale MOSFET device physics. The source-channel barrier played a key role in our discussions. Note, however, that it is possible to compute the ballistic I-V characteristic without reference to this barrier. The key quantity is $n_S(V_{GS})$, which can be computed for an MOS capacitor in equilibrium, then shifted in voltage to account for short-channel effects. Modulation of the source-channel barrier height is what provides inversion charge to balance the gate charge. Our assumption that +k-states at the top of the barrier are populated according to the source Fermi level removes the need to treat transport over the barrier explicitly (much like the "Law of the Junction" for a bipolar transistor). In practice, transport across the barrier will be less than perfect, and the effect will appear as a series resistance in the device.

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