The Use of a Green's Function Formalism for the Simulation of Semiconductor Device Performance

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ABSTRACT

Non-equilibrium quantum transport simulation techniques (e.g. the generalized Kadanoff-Baym approach) have been in existence for over 40 years but have only recently become numerically viable for the simulation of semiconductor devices. This paper reports on Motorola's effort at building a quantum transport device simulator suitable for the predictive quantum-mechanical simulation of MOSFETs beyond the $L_{eff} = 100nm$ technology-node.

Keywords: quantum transport, non-equilibrium green functions, kadanoff-baym, device simulation, mosfet

1 INTRODUCTION

The semiconductor industry has arrived at the point where quantum-mechanical effects are having a major influence on the device design process. As a result, device simulators built around nonequilibrium quantum transport theory have recently appeared which address many of the emergent quantum mechanical issues. Such simulators enable both the continued optimization of near-term process technologies and will ultimately serve as innovation platforms for the development of future (opto)-electronic and molecular devices.

A major constraint for quantum transport simulators is that they properly incorporate scattering processes to accurately capture realistic device performance at room temperature. Furthermore, the framework must simulate general (nonequilibrium) biasing conditions while suitably representing the electronic bandstructure within the relevant material systems. The theory of choice for such an implementation is the Kadanoff-Baym (K-B) formalism[1]–[4], often referred to as the nonequilibrium Green's functions (NEGF) method.

2 KADANOFF-BAYM FORMALISM

The K-B formalism has been analytically applied to numerous nonequilibrium transport problems since it's inception in the early 1960s. K-B theory involves solving transport equations for non-equilibrium Green's functions which encompass the retarded (G^r) and advanced (G^a) Green's functions, and the particle ($G^<$) and hole ($G^>$) correlation functions. Of the full set of NEGFs, only two are independent (typically chosen to be G^r and $G^<$) which necessitates solution of the following spatially discretized steady-state transport equations;

$$[E - \mathbf{H} - \mathbf{\Sigma}^r]\, \mathbf{G}^r = \mathbf{I}, \tag{1}$$

$$[E - \mathbf{H} - \mathbf{\Sigma}^r]\, \mathbf{G}^< = \mathbf{\Sigma}^< \mathbf{G}^a, \tag{2}$$

where the bold quantities denote matrices in the discretized coordinates, $\mathbf{\Sigma}^r$ is the particle scattering rate, and $\mathbf{\Sigma}^<$ accounts for particle in-scattering. All physical quantities of interest for particles (electrons) and holes, including densities, currents, transmission characteristics, etc., can be generated directly from $G^<$. The primary difficulty in solving K-B problems numerically stems the fact that Eqs. 1-2 are matrix equations with pathological scaling properties in the spatial dimensions. When scattering is incorporated into the model, the K-B equations can easily become intractable.

2.1 Numerical Implementation for MOSFET Simulation

It is only recently, with the availability of advanced computing platforms, that numerical implementations of the K-B formalism have been developed for a number of device problems[5], [6]. To facilitate the modeling of contemporary scaled MOSFETs, we have implemented a two-dimensional (2D) K-B-based quantum transport simulator which self consistently couples many-body effects (local density approximation) with scattering. Our model uses a single band effective mass Hamiltonian with multiple, independent valence- and conduction-band valleys to optimize the matrix structure of the K-B transport equations. The resulting Hamiltonian is sparse block-tridiagonal which enables the use of efficient recursive algorithms for the solution of Eqs. 1 and 2.

The treatment of scattering, which is essential for the accurate modeling of device behavior and scaling properties, is achieved through an empirical model whereby $\mathbf{\Sigma}^r$ is calibrated to reproduce quasi-equilibrium effective mobility (μ_{eff}) data. This enables the efficient treatment of the primary bulk and interface scattering mechanisms present in typical MOS material systems. However, with this model, $\mathbf{\Sigma}^<$ must be chosen carefully

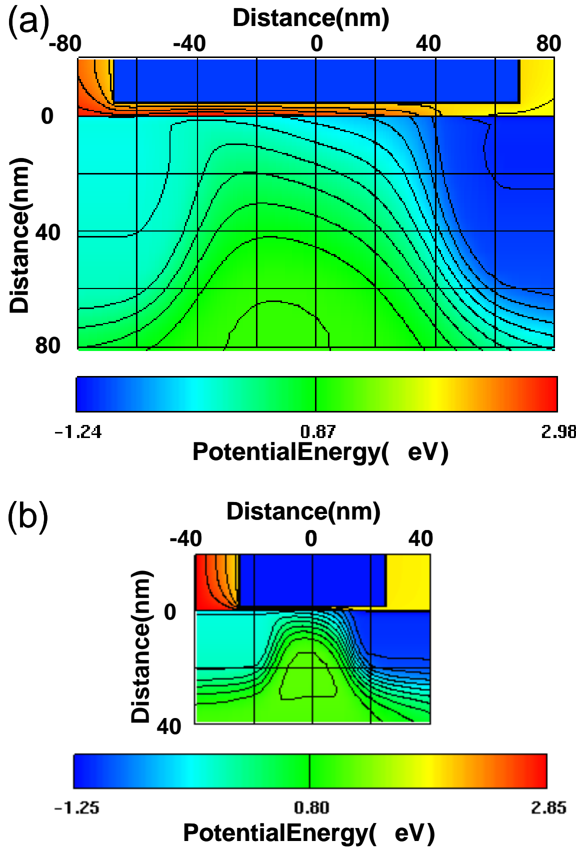

Figure 1: Self-consistent conduction band (potential energy) profiles for the (a) $L_{eff} = 90nm$ and (b) $L_{eff} = 25nm$ MIT reference MOSFETs.

to satisfy particle conservation. This is accomplished by forcing $\mathbf{\Sigma}^{<}$ to obey

$$\mathbf{\Sigma}^{<} = \frac{Im\left[\mathbf{\Sigma}^{\mathbf{r}}\right]}{Im\left[\mathbf{G}^{\mathbf{r}}\right]}\mathbf{G}^{<} + \boldsymbol{\sigma}^{<}, \tag{3}$$

which ensures global current continuity at the expense of added complexity in Eq. 2. In Eq. 3, a distinction is made between particle scattering (first term on r.h.s.) and contact injection ($\boldsymbol{\sigma}^{<}$) to illustrate that contact injection is also handled through the self-energies.

3 RESULTS

In order to provide insight into existing and future MOSFET performance, we performed both quantum transport and semi-classical (drift-diffusion) simulations of the MIT $L_{eff} = 90nm$ and $L_{eff} = 25nm$ MOSFETs[7]. The relative scale and self-consistent potential energy profiles of these devices under saturation bias ($V_{GS} = V_{DS} = 1.0V$) is illustrated in Fig. 1 for reference.

Prior to the simulation of full MOSFETs, a detailed calibration of our empirical scattering model was performed against experimental data. Since the physics of the MOS interface requires a comprehensive treatment of both bulk and interface scattering processes, we performed our calibration against effective mobility (u_{eff}) - effective field (E_{eff}) data. The results of the calibration, illustrated in Fig. 2, demonstrate the good agreement achieved between our empirical scattering model and experimental data[8].

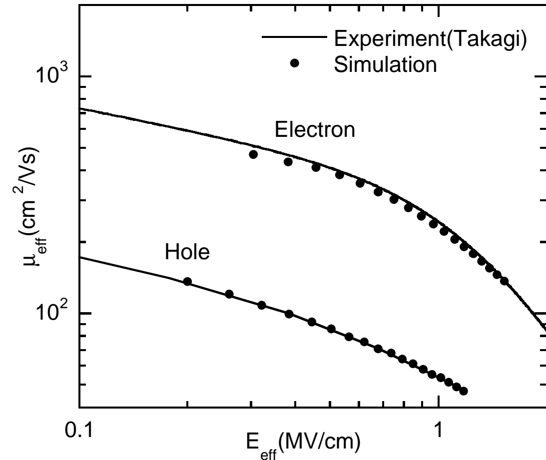

Figure 2: Simulated effective mobility (μ_{eff}) vs. effective field (E_{eff}) curves generated from the calibrated scattering model

We subsequently tested this model within our full quantum transport simulator and compared the results against drift-diffusion theory and experimental data for the $90nm$ MIT MOSFET. Although possessing a short L_{eff}, the $90nm$ MIT MOSFET has a relatively large SiO_2 thickness ($t_ox = 4.5nm$), which minimizes the impact of quantum effects and makes this an essentially semiclassical device. The results of the comparison (illustrated in Fig. 3) show good agreement between quantum transport and semiclassical theory and both sets of data match well with the available experimental data. This suggests both that quantum-transport simulators can effectively simulate realistic device performance and that semi-classical models are still valid for device technologies on the scale of the $90nm$ MOSFET. However, future device scaling is expected to make quantum effect more prominent in device operating characteristics and existing semi-classical models are expected to be rendered invalid. We test out these predictions in the following section.

4 DISCUSSION

MOSFET scaling requires the simultaneous reduction in oxide thickness (t_{ox}) and gate-length (L_{poly}) to achieve sequential improvements in process technology performance. Presently, devices with $t_{ox} = 2nm$ and

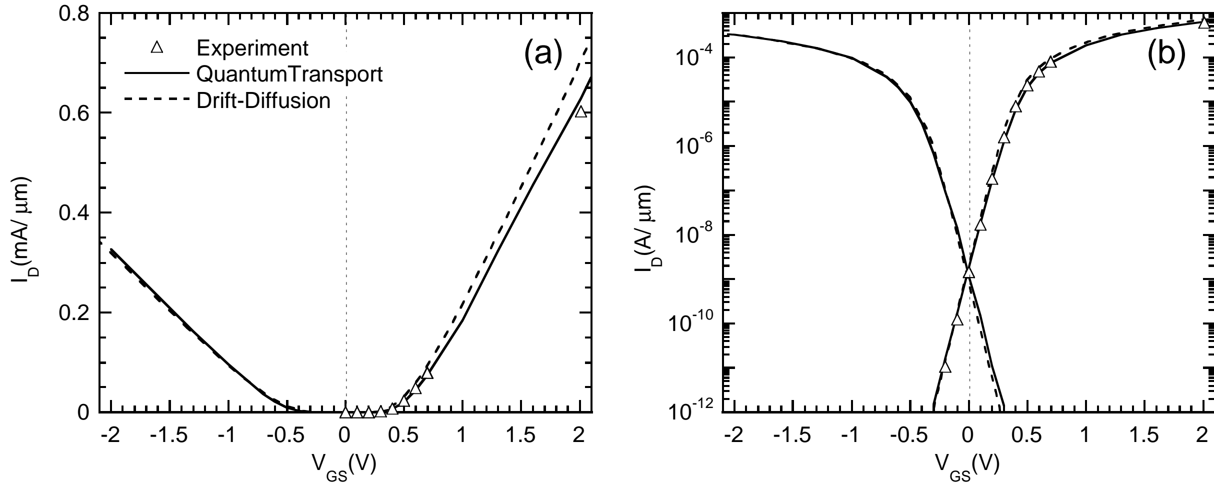

Figure 3: Comparison of (a) linear and (b) log quantum-transport and drift-diffusion simulated I_D-V_{GS} characteristics for the $90nm$ MIT MOSFET under saturation ($V_{DS} = 1.0V$). Experimental data for for the nMOS transistor is shown for reference.

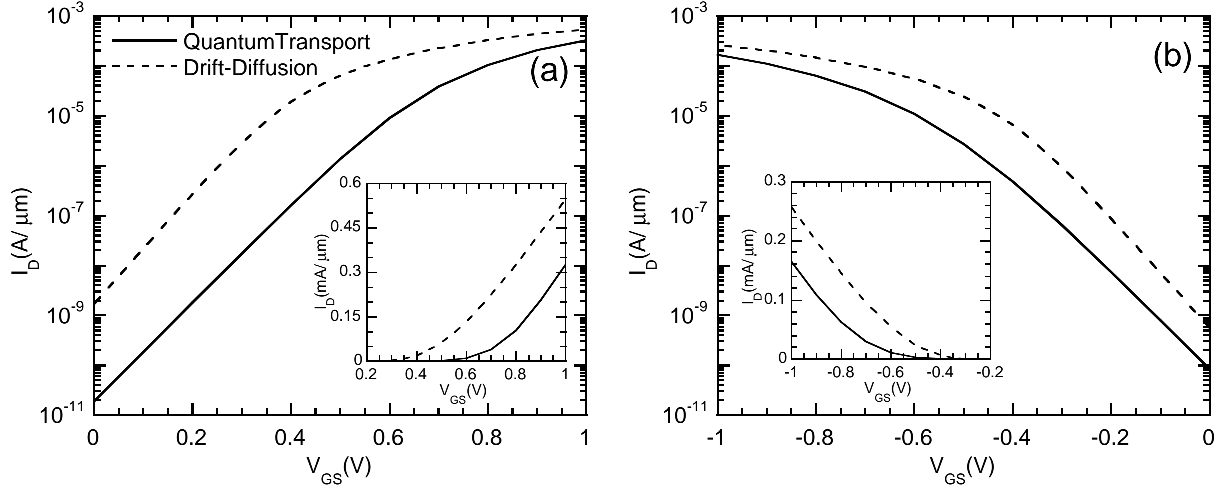

Figure 4: Comparison of quantum-transport and drift-diffusion simulated I_D-V_{GS} characteristics for the $25nm$ MIT MOSFET under saturation bias ($V_{DS} = 1.0V$). Both (a) nMOS and (b) pMOS transistor data is shown

$L_{poly} = 90nm$ are entering production and devices with significantly smaller values t_{ox} and L_{poly} are under development. To gain an understanding of the degree to which quantum effects will influence future technologies, we examined two effects using our simulator; the quantum-mechanically induced threshold voltage (V_t) shift and the impact sub-threshold tunneling on device leakage.

4.1 Quantum-Mechanical V_t Shift

A manifestation of any quantum-mechanical system with a step-boundary or interface (e.g. the $Si - SiO_2$) is that the charge density in the vicinity of the interface will be depleted. This effect arises from the fact that the charge density is constructed from wave-functions which display analytic behavior (i.e. continuity) across interfaces. Consequently, there is a shift in the induced charge centroid away from the interface resulting in a decreased effective oxide capacitance (C_{ox}). For present-day process technologies with $t_{ox} < 2.5nm$, the capacitive loading of the centroid shift can be significant. This is illustrated in Fig. 4 which compares quantum-transport and semi-classical simulations of the $25nm$ MIT MOSFET ($t_{ox} = 1.5nm$). The impact of interfacial charge depletion on this technology leads to a predicted $0.2V$ (0.1) nMOS (pMOS) V_t shift from the semiclassical

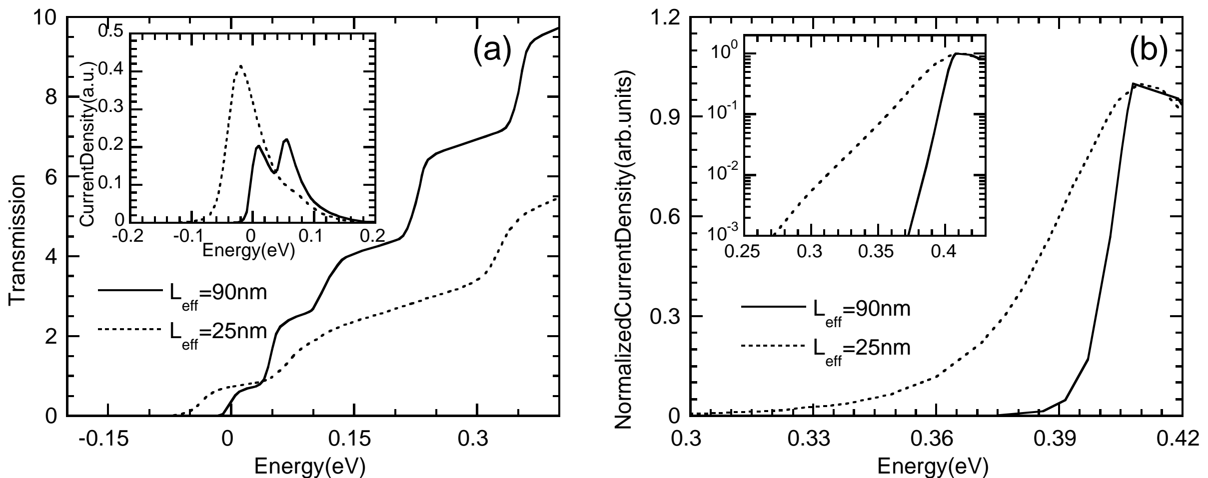

Figure 5: Comparison of (a) saturation transmission characteristics and (b) normalized current density for the $L_{eff} = 90nm$ and $L_{eff} = 25nm$ MIT MOSFETs

model data. Clearly, the incorporation of this effect in semiclassical device simulators is vital to their continued use in technology simulation and efforts are already underway to augment semiclassical models with effective quantum potentials[9].

4.2 Sub-Threshold Tunneling

An additional issue impacting scaled MOSFETs is onset of tunneling through the channel barrier when the device is biased in the off-state ($V_{GS} = 0V, V_{DS} = V_{DD}$). Again, this is a mechanism that can be generally ignored for contemporary technologies but which may become significant in future scaled devices. To assess it's potential impact, the transmission characteristics and current density for the $90nm$ and $25nm$ MOSFETs are compared in Fig. 5.

As carriers flow through a MOSFET, they are confined to subbands due to the gate-induced potential and subsequently display a step transmission spectrum (Fig. 5(a)). In the off-state, a source-drain potential barrier is designed to be an impediment to carrier transport thereby allowing the MOSFET to switch off. However, as illustrated in Fig. 5(b), devices with $25nm$ can have a substantial current-density tail which indicates the presence of tunneling through the source barrier. For the $25nm$ device, the sub-threshold tail accounts for about 50 % of the off-state current and this component can be expected to increase exponentially as device technologies scale further.

5 CONCLUSION

We have demonstrated that the K-B formalism is both a tractable and predictive simulation technique for the simulation of present and future semiconductor technologies. With suitable modifications to the underlying Hamiltonian and scattering models, the K-B approach should see substantial use for the simulation of future novel devices technologies. This trend will undoubtedly be accelerated by the rapid developments in commodity computing platforms which will make the K-B universally accessible for device simulation in the near future.

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