Methodology for Model Generation with Accuracy from DC to RF

Xisheng Zhang, Mark Williams, Zhihong Liu

Celestry Design Technologies, Inc.
1982A Zanker Road, San Jose, CA 94087

ABSTRACT

This paper presents an example modeling flow for generating a RF CMOS model. Initially, the objectives of this modeling approach are analyzed. Then issues in test structure design are discussed. In the section of model generation, we cover the procedures of DC, AC, 1/f noise and RF modeling. We examine the issues related to measurement, parameter extraction, and optimization. We then focus our discussion on the issues related to advanced CMOS technology: gate tunneling current, measuring gate capacitance with high tunneling current, and de-embedding in s-parameter measurement. We present a method to determine the ratio, between drain and source, of the gate to channel tunneling current. We also briefly introduce the 1/f noise measurement system, which can do on wafer 1/f noise characterization. Finally, we present the fitted model results.

Keywords: CMOS, RF, measurement, parameter extraction, SPICE model

INTRODUCTION

Advances in wireless design demands a compact model that can accurately predict MOSFET behavior at DC and high frequency [1,2]. This is critical for the first pass design success and for meeting the marketing window of RF CMOS product. We will present an example modeling flow for generating a model that can meet these requirements. Our presentation is as follows: We begin with a brief discussion on the basic requirements of this kind of model. Next we present some guidelines to design the test structures. After that, we discuss the procedures of model generation: DC modeling, AC modeling, noise modeling and RF modeling. Each procedure includes the measurement, extraction, optimization and model validation steps.

We use the BSIM4 model as an example. The devices are NMOSFET, with minimum channel length (L=0.18um).

MODEL OBJECTIVES

There are a number of goals with regard to predicting the accurate behaviors of a device. The following is a list of suggested considerations when generating a broad range model.

- DC behavior - These include the terminal currents, their derivatives and temperature effects. Note, the first order derivatives of drain current (Gm, Gds) are directly related to fitting of Y_{21} and Y_{22}.
- Frequency domain behavior - These include the gate capacitances, junction capacitances and their temperature effects.
- Small signal parameters at high frequency.
- Nonlinear behavior – required for accurate simulation of distortion or circuits containing VCO's.
- Noise - There are two major noise mechanisms in a MOSFET: thermal noise and 1/f noise. 1/f noise is also important in RF design: one example is its influence to phase noise of VCO [3].
- Scalability verses channel length, channel width and finger number.
- Model for reliability simulation (HCI, NBTI)

Our work covers the area of DC, AC, 1/f noise and small signal parameter modeling.

TEST STRUCTURE DESIGN

The s-parameters are typically measured from a two-port network layout structure, with port one connected to gate and port two connected to drain. The body and source are normally connected to ground. This structure cannot be used for DC modeling, hence the DC and RF test structures need to be separately designed.

In a DC test structure design, there are two major issues: (i) when using the common gate, common source layout, the layout of the test devices must be optimized so that the devices with lower channel resistance are closer to the common pads, and (ii) for very short channel devices (L<0.15um), the Kelvin structure needs to be used to get an accurate measurement.

AC test structures should include the gate capacitance structure and junction capacitance structure. For the gate capacitance structure, a single device layout (without common gate/source) must be used. For the junction capacitance structure, structures with large area and long periphery are required for extraction of Cj and Cjsw related parameters. Optionally, one can layout the junction in the gate area to extract the sidewall capacitance at gate side.

The 1/f noise can be measured using DC test structure.

S-parameter measurement requires special probes. Depending on the type of probe, the pad of test structure can be laid out as G-S-G or G-S. Our experience shows that G-S-G is better since the measurement is more stable. The major issue in S-parameter measurement is de-embedding. Since CMOS transistors are fabricated in a relatively high conductive substrate, de-embedding is essential for an accurate s-parameter measurement. There are many de-embedding methods available [4]. The layout of a dummy structure is methodology dependent. Potentially, the dummy structures should include dummy open, dummy short, dummy through and pad only structure. Based on our experience, for designs less than 5 GHz, the dummy open and dummy short structure are adequate. The de-embedding procedure will be further discussed in high frequency modeling section.

MODEL GENERATION

The procedure for model generation should start from DC modeling since it predicts the operation points of a device. After DC modeling, one should consider AC modeling, RF modeling and Noise modeling. Each step of modeling includes measurement, parameter extraction, optimization, and model validation. Since the model generation is a quite complicated process, we will not discuss all the issues in this paper, but rather focus on the new issues in today's technologies.

DC modeling

Physical extraction is the key step in developing a scalable RF model. In additional to traditional physical extraction methods [5], we have to take into account the gate tunneling current in today's technologies. There are five tunneling components: tunneling current from gate to drain, source and bulk, tunneling current from gate to channel then to source or drain. To do the gate current measurement, it is desirable to choose devices with large area. The first three tunneling components can be easily measured. The last two components cannot be measured directly. The gate to channel tunneling current can be obtained from measurement. The partition of current from channel to source and from channel to drain needs to be extracted. We propose the following procedure: first, the gate to channel tunneling current at Vds=0 should be measured, where Vds is drain to source voltage drop. Then the gate to channel tunneling current at different Vds's should be measured. BSIM4's formula of Igcs,tunnel and Igcd,tunnel are:

$$I_{gcs,\,tunnel} = I_{gc0} \times \frac{-1 + PIGCD * Vds + e^{-PIGCD \times Vds} + 10^{-4}}{(PIGCD \times Vds)^2 + 2 \times 10^{-4}} \quad (1)$$

$$I_{gcd,\,tunnel} = I_{gc0} \times \frac{1 - (PIGCD * Vds + 1) \times e^{-PIGCD \times Vds} + 10^{-4}}{(PIGCD \times Vds)^2 + 2 \times 10^{-4}} \quad (2)$$

where PIGCD is the ratio of Igc partition, Igc0 is gate to channel measured at Vds=0. PIGCD is the ratio we need to extract.

Assume at Vds=Vdmax, PIGCD*Vds >>10^{-4}, then we get

$$\frac{I_{gcs,\,tunnel} + I_{gcd,\,tunnel}}{I_{gc0}} \approx \frac{1}{PIGCD * Vds} \quad (3)$$

The PIGCD can be estimated from the ratio of Igc(Vds=Vdmax)/Igc(Vds=0). A more accurate PIGCD value can be extracted from least-square fitting of Igc measured at different Vds. Figure 1 is fitting result of gate current (the points are the measurement results, the line is BSIM4 simulation result). BSIM4 model can provide a good fitting of gate tunneling current.

AC modeling

To measure the gate capacitances, we have to connect the gate to low terminal of LCR meter in order to reduce the noise pickup. Since the gate has been connected to ground, the biases of other terminals have to be adjusted accordingly. Figure 2 is the measurement setup for measuring gate to drain capacitance.

For very thin gate oxide, there is an effective resistance due to the gate tunneling current. To measure gate capacitance in this circumstance, we have to use the two frequencies to perform the CV measurement [6].

Note: we are using the capmod=2 in BSIM4 model.

1/f noise modeling

Figure 3 is the measurement setup for 1/f noise measurement. Compared with traditional measurement setup, the biasing of the device is done using a regular IV meter. The advantage of this setup is we can use software to change the bias of device, thus one can easily do batch mode measurement. Special noise filters have been added to reduce the noise floor. The system noise floor is less than $2x10^{-26}A^2/Hz$. This system can also do the on-wafer measurement. Figure 4 displays the measured 1/f noise at different temperatures.

Note: we are using the noimod=2 in BSIM4 model.

RF modeling

S-parameter measurement is significantly more complicated. In additional to a calibration procedure, de-embedding is a must in RF CMOS modeling. This is largely because the measured data contains parasitics brought about by the test structure itself. Things such as pad and metal line parasitics need to be removed before the data can be used for modeling. Data collected from the Open test

structure mainly suffers from parallel parasitics. The data from the Shorted test structure suffers from both parallel and series parasitics. Thus, Open and Short test structures can be used in tandem to calculate the separate contribution of parallel and series parasitics. These can then be used to de-embed (Figure 5) all parasitics from the data measured using the Device Under Test (DUT) test structure.

The purpose of physical extraction is to provide a good initial guess for the subsequent optimization of the model parameters. To carry out this extraction process, the technique from [2] is used with some modifications. Its small-signal equivalent circuit is used to derive mathematical expressions for the four parameters y_{11}, y_{12}, y_{21}, and y_{22}. Quasi-static approach has been used [2].

Some of the previous model parameter values determined by physical extraction can be changed in order to achieve even better fitting accuracy between measured and simulated y-parameter characteristics. This optimization process provides a unique challenge to RF CMOS model extraction because of the sub-circuit nature of the model. The introduction of so many extrinsic elements really means that we are optimizing a circuit (albeit a small one) in contrast to a single device used in traditional low-frequency modeling. We are using a modified SPICE engine for a fast RF simulation and optimization [7].

Table 1 lists a recommended collection of parameters that can be optimized and their intended targets.

Parameters	Fitting Targets
R_g	$Re(y_{11})$
R_{dsb}, R_{sb}, R_{db}	$Re(y_{22})$ and $Im(y_{22})$
C_{gso}	$Im(y_{11})$
C_{gdo}	$Im(y_{12})$, $Im(y_{21})$
C_{gbo}	$Im(y_{11})$, $Im(y_{12})$, $Im(y_{21})$

Table 1. Different model parameters are used to fit different y-parameters.

Figure 6-8 shows the fitting results for a one scaleable model. Figure 6 shows fitting of s-parameters at different biases (the finger number is 32). Figure 7 shows Ft fitting at different biases for a finger number equal to 64. Figure 8 shows Ft fitting for a finger number equal to 16.

CONCLUSIONS

An example RF CMOS modeling flow has been presented. This flow should include the DC, AC, RF and noise modeling steps. Some special issues related to very short channel device modeling have been discussed. We have shown that BSIM4 can fit gate tunneling current quite well. When measuring the gate capacitance, the gate tunneling current must be considered. In RF modeling, the de-embedding is essential to ensure the quality of measurement data. BSIM4 can provide a good scalable model verse different finger number.

ACKNOWLEDGENT

This paper is a summary of recent research and development work done in Device Modeling Division of Celestry Design Technologies, Inc. Dr. Ping Chen and Dr. Jushan Xie contributed the part of BSIM4 modeling. Jim Zhao contributed the part related to CV measurement. Dr. Weiquan Zhang and Dr. Hancheng Liang contributed the part related to RF modeling. The authors wish to thank them for their contribution and support.

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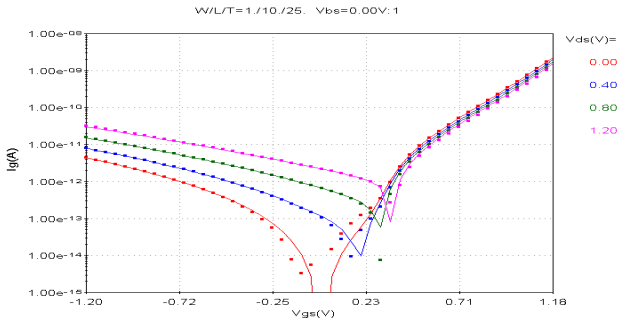

Fig.1. Fitting result of gate tunneling current at different bias.

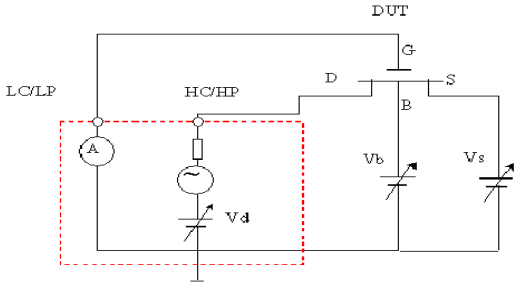

Fig.2. Setup for measuring gate to drain capacitance.

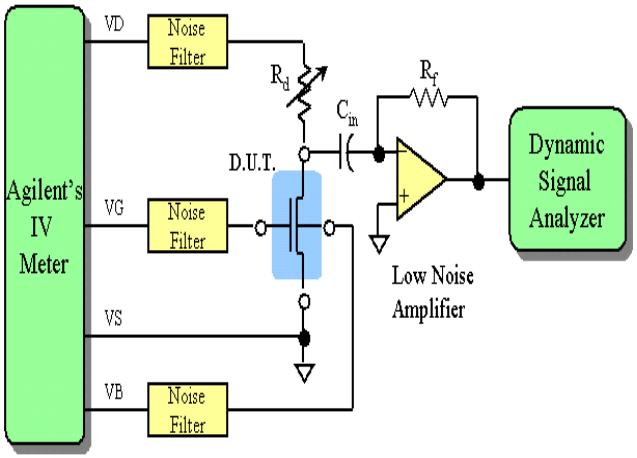

Fig.3 1/f noise measurement setup

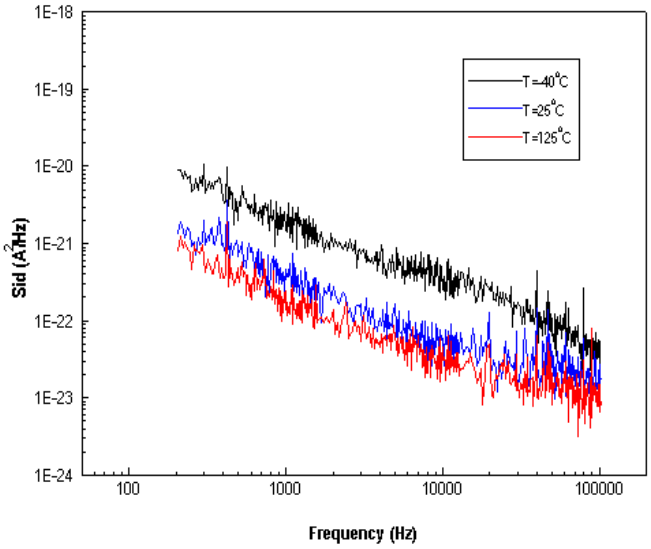

Fig.4 Measured 1/f noise for device W/L=20/0.35

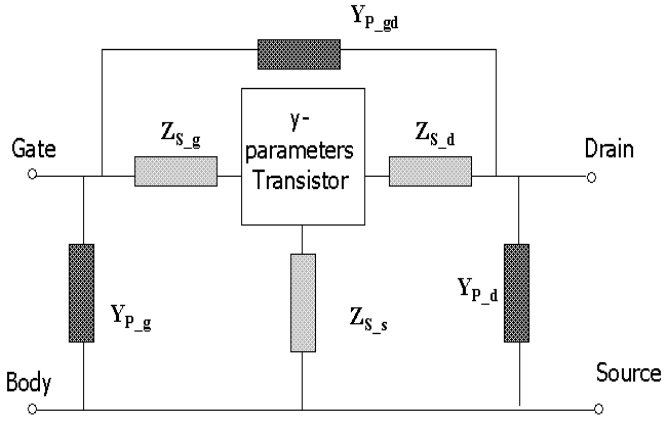

Fig.5. Equivalent circuit diagram used for the two- step de-embedding

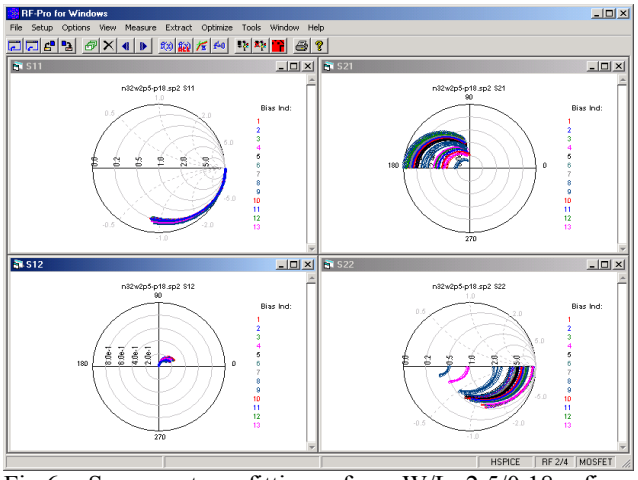

Fig.6 S-parameter fitting for W/L=2.5/0.18 finger number=32

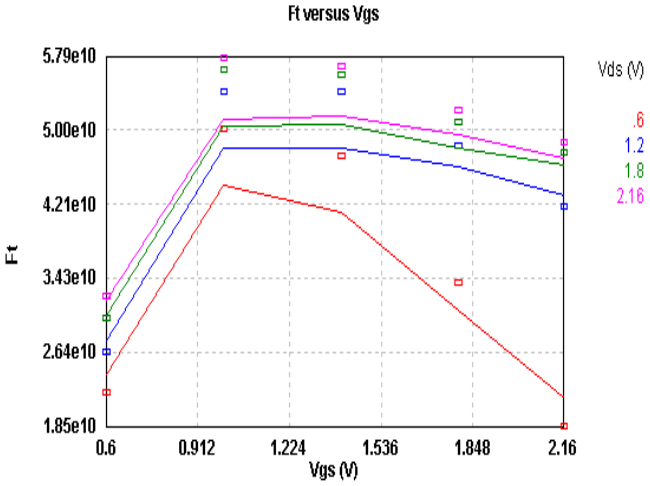

Fig. 7 Ft fitting for W/L=2.5/0.18 finger number =64

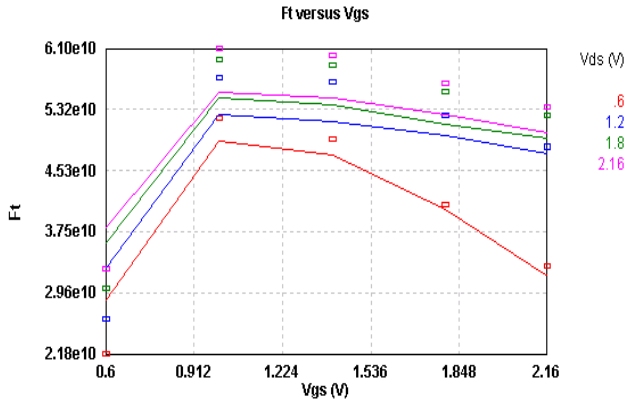

Fig.8. Ft fitting for W/L=2.5/0.18, finger number=16