# Measurements and modeling of mobility in ultra-thin SOI

M.Mastrapasqua*, D. Esseni** and C.Fiegna***

* Agere Systems, 600 Mountain Ave, Murray Hill NJ, USA, mastrapasqua@agere.com
** DIEGM - Univ. of Udine, Via delle Scienze 208, 33100 Udine, Italy, esseni@uniud.it
*** Dept. of Electrical Engineering - University of Ferrara, Italy, cfiegna@ing.unife.it

## ABSTRACT

We present a study of the effective mobility ($\mu_{eff}$) of ultra-thin SOI n-MOSFETs for both single and double gate operation. Electron mobility was measured for silicon thickness $T_{Si}$ down to approximately 5 nm using a special test structure able to circumvent parasitic resistance effects. At small inversion density, $N_{inv}$, the mobility is clearly reduced for decreasing $T_{Si}$, due to enhanced phonon scattering in the thin quantum well. However, for double gate operation, DG, we found an improvement in the effective mobility when compared with single gate, SG, operation.

***Keywords***: SOI, mobility, ultra-thin SOI, fully depleted, quantization.

## 1 INTRODUCTION

Fully depleted SOI MOSFET have been indicated as the selected choice for the scaling of CMOS below the 50 *nm* node [1]. Modeling of FD-SOI transistors poses considerable challenges, due to the complex behavior of the depleted body and due to the carrier transport in the thin silicon layer with two oxide interfaces. Moreover, for silicon thickness below 15 *nm* quantum confinement effects are affecting not only the transistor threshold value [2] but also the carrier transport itself [3]. In this work we present experimental data on the inversion-layer mobility in silicon layers in the 5–50 nm range. The mobility curves in the single-gate operation mode at high inversion concentrations are shown to agree with bulk results, so that conventional mobility models can be employed. For thin silicon layers, a mobility degradation is observed at low inversion densities. However, a mobility enhancement is found for DG operation.

## 2 DEVICE FABRICATION

Device processing started with Unibond SOI wafers produced by the Smart Cut process and featuring a 200 nm (100) Si film over 400 nm buried oxide. The Si film was thinned down to 9, 13, 20, and 60 nm nominal thickness through a series of oxidations at $1000^oC$ followed by etching of the sacrificial oxide. Typical thickness control was 2 nm across the wafer that is about 25% variation of $T_{Si}$ for the thinnest SOI, still acceptable for our study because $\mu_{eff}$ and $T_{Si}$ were accurately measured on the same device. Local oxidation (LOCOS) tailored to consume the entire Si film, provided lateral isolation. After LOCOS, simplified processing of NMOS and PMOS devices was adopted: transistor channels were left undoped (p-type 10 Ohm-cm resistivity), there was no LDD implant and no spacer formation. The energies of the S/D implants were adjusted to the different $T_{Si}$ values. Gate oxide thickness $T_{ox}$ was 4.5 nm.

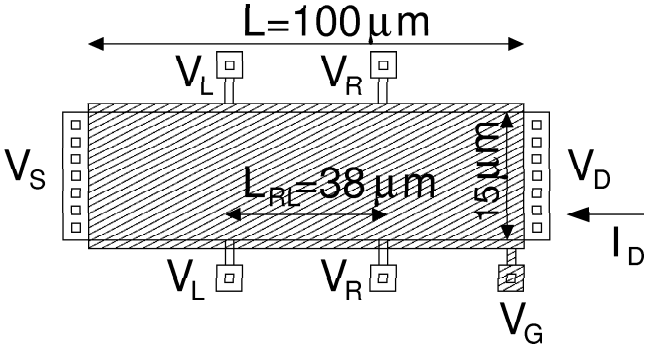


Figure 1: Schematic top-view of the MOSFETs used for $\mu_{eff}$ measurements. $V_R$ and $V_L$ were measured at the voltage probes and used to determine the exact intrinsic drain to source voltage $V_{DS}^{(int)} = (L/L_{RL}) \times (V_R - V_L)$ independent of possible series resistances.

## 3 MEASUREMENTS TECHNIQUES

Fig. 1 shows a schematic top-view of the specially designed MOSFETs used for $\mu_{eff}$ measurements. The structure is symmetrical with respect to the channel length direction and two pairs of voltage probes allow us to measure $V_R$ and $V_L$ within the channel. Mobility is calculated as $\mu_{eff} = (L/W) \times (g_d^{(int)}/qN_{inv})$ where $g_d^{(int)} = [I_{DS}/V_{DS}^{(int)}]$ with $V_{DS}^{(int)} = (L/L_{RL}) \times (V_R - V_L)$. $(V_D - V_S)$ was adjusted to maintain $V_{DS}^{(int)} \simeq 10mV$ for all measurements. We verified that the measurement results are unaffected by either switching the two pairs of probes or by contacting both pairs at once. As a result, although devices showed high source/drain resistance $R_{SD}$, due to the absence of elevated contact

structures, this four-probes measurement technique is unaffected by $R_{SD}$.

Due to inevitable processing spread associated with oxidation and etch used to thinning the silicon layer, a range of final $T_{Si}$ values was found within each wafer. Therefore the characterization technique of [4] was employed to extract an electrical $T_{Si}$ on the same device structure used to measure $\mu_{eff}$. A large back-gate bias ($V_{BG}$) was applied to invert the silicon back interface. Then CV measurements were performed by sweeping the front gate bias $V_G$ down to negative values to switch off the front inversion layer. Under these conditions one can access the back inversion layer through the series of the front gate oxide and the silicon thin film capacitance so that the silicon thickness can be easily extracted [5].

For SG operation, $N_{inv}$ was determined directly through gate-channel CV measurements [6] at a frequency ($5kHz$) low enough to avoid the influence of the channel resistance on measured capacitance. When SOI transistors are biased in DG operation with generic $V_{FG}$ and $V_{BG}$ values the experimental determination of $N_{inv}$ is not straightforward [7]. To this purpose we define $C_{FG} = q\partial N_{inv}/\partial V_{FG}$ and $C_{BG} = q\partial N_{inv}/\partial V_{BG}$, and then we can express $N_{inv}$ as a function of $V_{FG}$ and $V_{BG}$ as:

$$N_{inv} = N_{inv}^{(0)}(V_{FG}^{(0)}, V_{BG}) + 1/q \int_{V_{FG}^{(0)}}^{V_{FG}} C_{FG}(V, V_{BG})dV \quad (1)$$

where $V_{FG}^{(0)}$ is a generic, initial value for the front-gate voltage and $N_{inv}^{(0)}$ is the corresponding inversion charge and depends on $V_{FG}^{(0)}$ and $V_{BG}$ . From Eq.1 we see that, for a given $V_{BG}$, if $V_{FG}^{(0)}$ is such that $N_{inv}^{(0)} \simeq 0$, then $N_{inv}$ can be obtained integrating the $C_{FG}$ curves similarly to conventional SG operation mode. Fig.2 reports measured $C_{FG}$ versus $V_{FG}$ characteristics for different $V_{BG}$. At relatively large, negative $V_{FG}$ the capacitance goes to zero because $V_{FG}$ can dismiss the inversion charge induced by the large, positive $V_{BG}$ so that the condition $N_{inv}^{(0)} \simeq 0$ is fulfilled [8].

Following the outlined procedure, the $N_{inv}$ values used for $\mu_{eff}$ extraction were obtained, for each $V_{BG}$, integrating the corresponding $C_{FG}$ as indicated in Fig.2 for both the SG and DG case. In order to verify this procedure, we note that when both $V_{FG}$ and $V_{BG}$ are well above the respective threshold voltages, then $C_{BG}$ is expected to equal the back-oxide capacitance $C_{box} = \epsilon_{ox}/T_{box}$ and to become independent of $V_{BG}$ and $V_{FG}$. Fig.?? reports $N_{inv}$ for $V_{BG}$ and $V_{FG}$ well above the corresponding threshold voltages. The $N_{inv}$ versus $V_{BG}$ linearity is virtually perfect and from the slope we can extract $C_{BG}$ and hence an effective $T_{box}$=407nm that is in close agreement with the nominal $T_{box}$=400nm and essentially independent of $V_{BG}$ and $V_{FG}$.

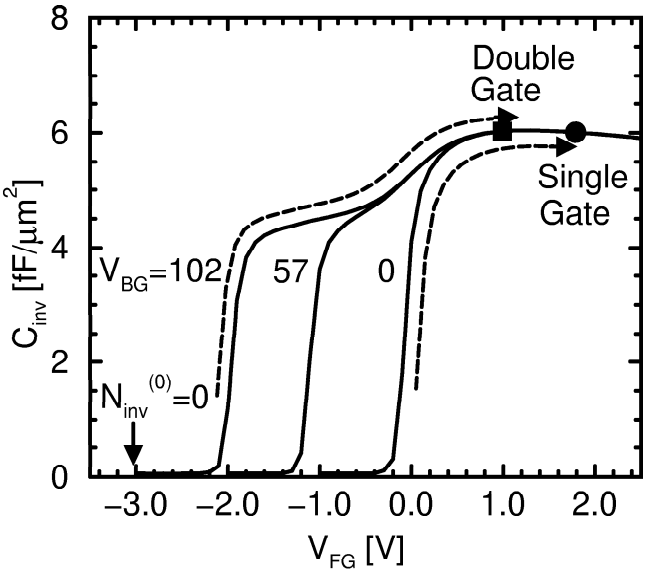


Figure 2: Measured $C_{FG}$ versus $V_{FG}$ characteristics for different back-gate voltages $V_{BG}$=0, 57 and 102V. The dashed arrows indicate the integrals performed to calculate $N_{inv}$ in either SG or DG operation mode. $T_{Si}$=9.4nm.

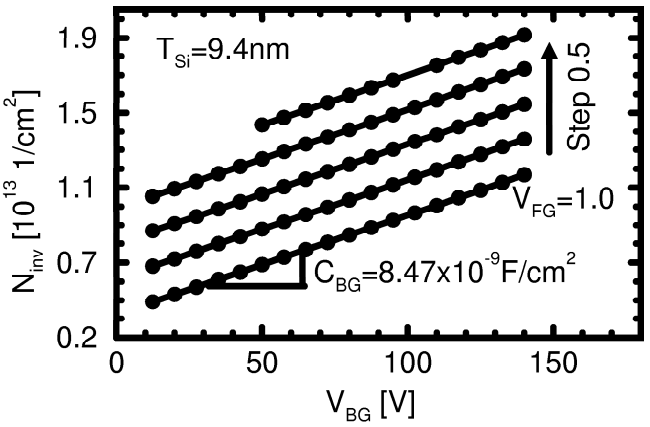


Figure 3: Measured $N_{inv}$ versus $V_{BG}$ for different $V_{FG}$. $N_{inv}$ is a linear function of $V_{BG}$ when $V_{BG}$ and $V_{FG}$ are above the respective threshold voltages. From the slope of the interpolating straight line we extract a $C_{BG}$ corresponding to an effective $T_{box}$ of 407nm, i.e. very close to the nominal $T_{box}$=400nm value.

## 4 DOUBLE vs. SINGLE GATE MOBILITY

Fig. 4 shows measured SG electron $\mu_{eff}$ for different $T_{Si}$ compared with data for bulk MOS [6] and previously reported SOI measurements [9], [10]. At high $N_{inv}$, $\mu_{eff}$ is largely insensitive to $T_{Si}$, consistent with $\mu_{eff}$ of low-doped bulk MOSFETs (filled circles) and it is remarkably larger than in heavily doped bulk devices (filled squares) due to the lower effective field in SOI devices. At relatively low $N_{inv}$, however, $\mu_{eff}$ is clearly reduced

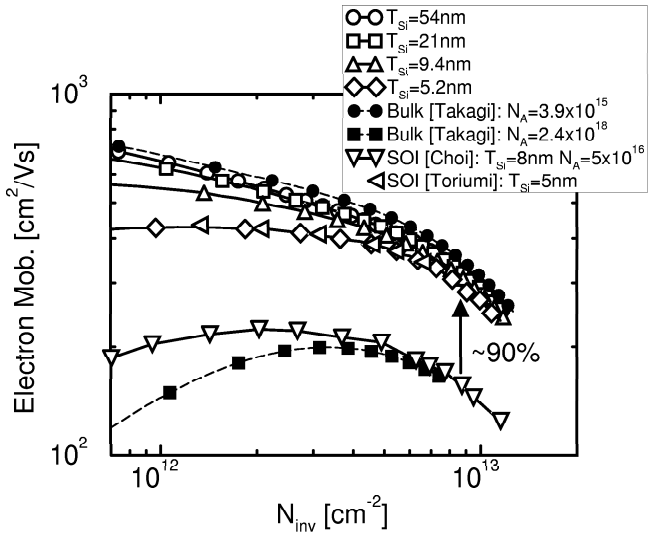


Figure 4: Measured room temperature electron mobility versus inversion charge density $N_{inv}$ for different $T_{Si}$ and SG operation.

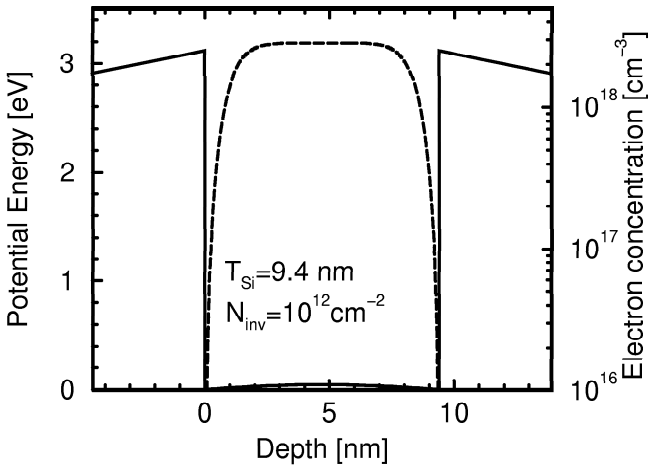


Figure 5: Simulated potential energy (solid line) and electron concentration (dashed line) versus the distance from the front Si-SiO2 interface in a DG bias condition. $N_{inv} = 10^{12}cm^{-2}$ indicates one half of the total inversion density. At this $N_{inv}$ a volume inversion is realized.

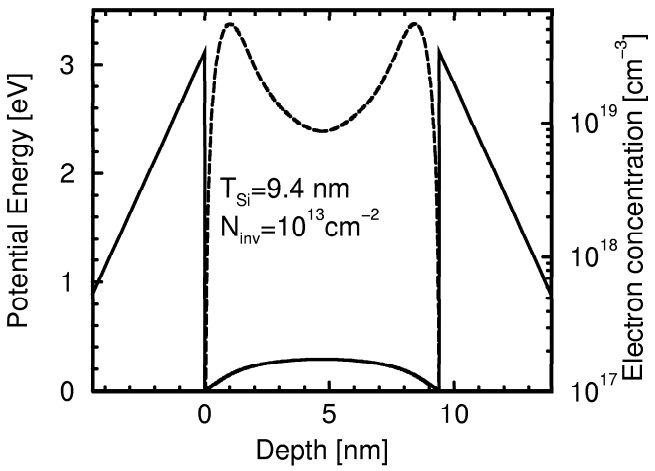


Figure 6: Simulated potential energy (solid line) and electron concentration (dashed line) versus the distance from the front Si-SiO2 interface in a DG bias condition. $N_{inv} = 10^{13}cm^{-2}$ indicates one half of the total inversion density. At this $N_{inv}$ two distinct peaks of the electron concentration

for $T_{Si}$ below $10nm$ and our data for $T_{Si} = 5nm$ are in very close agreement with those shown in [10]. On the contrary, mobility data reported by Choi et al. [9] are significantly lower than ours, possibly indicating a poor quality of the silicon layer [9]. The decrease of mobility at low $N_{inv}$ for thin silicon film was predicted by Gamiz et al. as a consequence of the increase in phonon scattering caused by electron confinement in the very thin silicon films [11].

In order to proceed with $\mu_{eff}$ measurements in DG mode, since in our samples $T_{box}$ is much larger than $T_{ox}$ (Fig.1), it is necessary to determine, for each $V_{FG}$, the $V_{BG}$ that realizes symmetrical charge profiles in the halves of the silicon film. To this purpose we used numerical simulations accounting for poly-depletion and subband quantization [12]. The energy diagrams and electron concentrations for two DG conditions corresponding to a charge density of $N_{inv} = 10^{12}$ and $10^{13}cm^{-2}$ are reported in Fig.5 and 6. (In the DG mode the indicated $N_{inv}$ is always one half of the entire inversion charge.) As can be seen, for $N_{inv} = 10^{12}cm^{-2}$ a volume inversion is found, that is the maximum of the electron concentration is at the middle of the silicon film. For $T_{Si} = 21$nm we measured virtually the same $\mu_{eff}$ in DG and SG mode, suggesting that for this $T_{Si}$ the two inversion layers are only weakly interacting and essentially represent two channels in parallel [13]. For smaller $T_{Si}$, instead, Fig. 7 clearly indicates a $\mu_{eff}$ improvement in the DG configuration.

## 5 DISCUSSION

The $\mu_{eff}$ improvement in the DG mode is larger at small $N_{inv}$ (where $\mu_{eff}$ is mainly limited by phonon scattering) and increases with decreasing temperature suggesting a modulation of the phonon scattering rate [13]. At high $N_{inv}$ (where $\mu_{eff}$ is limited by surface roughness scattering) practically no difference is observed between $\mu_{eff}$ in SG or DG mode. Fig.8 reports $\mu_{eff}$ for different symmetry conditions where the parameter $E_R$ is calculated by means of simulations as the ratio between the surface field at front and back-interface, hence $E_R$=1.0 in the DG condition. When we move from the front-channel to the back-channel oper-

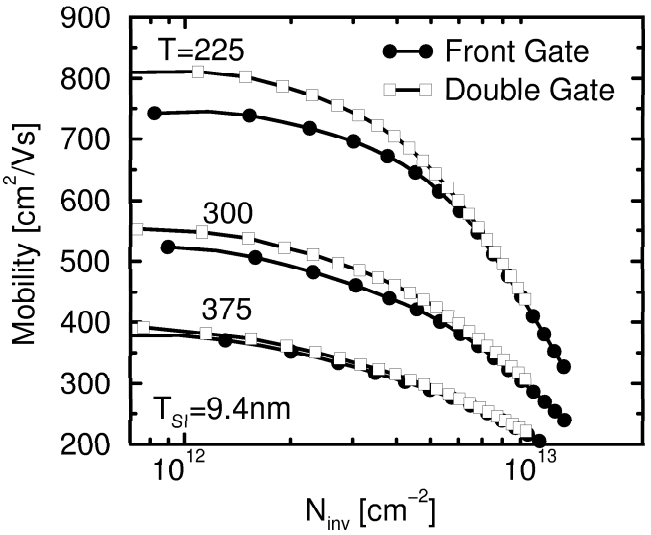


Figure 7: Measured mobility versus inversion density in either SG or DG mode for $T_{Si}$=9.4nm. A clear $\mu_{eff}$ improvement is observed in the DG mode at low $N_{inv}$. This effect is more pronounced for decreasing temperatures. In DG mode $N_{inv}$ indicates one half of the total inversion density.

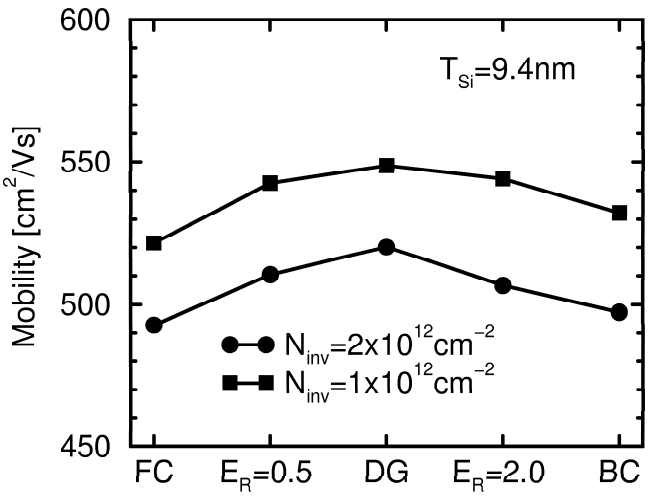


Figure 8: Measured mobility at two given inversion densities and different symmetry conditions. $E_R$ is the ratio of the surface field at the front and back-interface. $N_{inv}$ is the total inversion density in the FC and BC case while it is one half of the total inversion density in the DG mode and for $E_R$=0.5 or 2.0. A maximum of $\mu_{eff}$ is observed in the DG configuration.

ating mode $\mu_{eff}$ exhibits a maximum in the DG configuration. A similar behavior for phonon-limited mobility in ultra thin SOI MOSFETs has been recently predicted by numerical simulations [13].

## 6 CONCLUSION

Electron mobility of ultra thin SOI transistors operated in single and DG mode has been experimentally investigated for $T_{Si}$ down to 5nm and temperatures between 225 and 375K. For $T_{Si}$ ≈20nm mobility is essentially the same in DG as in SG mode. For thinner silicon films, however, at small $N_{inv}$ we observed a clear $\mu_{eff}$ improvement in DG mode that increases for decreasing temperatures. The models for low-field mobility implemented in conventional device simulators do not correctly account for the dependence on the thickness of the silicon layer in single and double-gate devices (Figs. 4 and 7; therefore, the development of a new advanced models for device and circuit simulators is mandatory. Such a model should explicitly relate the mobility to the 2-D subband structure in the inversion layer that is influenced by the silicon thickness due to strong size-induced confinement.

## 7 ACKNOWLEDGMENTS

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