

# CMOS RF Modeling and Parameter Extraction Approaches Taking Charge Conservation into Account

Minkyu Je, Ickjin Kwon, Jeonghu Han, Hyungcheol Shin, and Kwyro Lee

Dept. of EECS, KAIST

Also with MICROS Research Center, KAIST

373-1, Kusong, Yusong, Taejon, 305-701, Korea, krlee@ee.kaist.ac.kr

## ABSTRACT

A charge conserving small-signal equivalent circuit with very simple and accurate parameter extraction method for a three-terminal CMOS RF model is presented. We found that significant errors in circuit performances can be obtained if charge conserving non-reciprocal capacitances are not properly considered. It is also found that one accurate large-signal  $I$ - $V$  model is enough to be used for DC, low-frequency analog, as well as RF circuit simulation

**Keywords:** CMOS RF modeling, parameter extraction, charge conservation.

## 1 INTRODUCTION

The construction of proper small signal models and extraction of their parameters is very important not only for device and circuit characterization but for the circuit design. Recently, many suggestions have been made to improve the prediction of high-frequency properties by simple modification to the conventional MOSFET equivalent circuits developed for low-to-medium frequencies. Several methods of extracting small-signal equivalent circuit parameters from the  $S$ -parameter measurement data have been reported [1]-[4]. But they require complex curve fitting and optimization steps, or don't consider charge conservation capacitance parameters, which are very important in intrinsic capacitance modeling [5]-[7]. In this paper, we propose a simple and accurate parameter extraction method for a three-terminal CMOS RF model with charge conserving capacitances. The simulation results with and without considering charge conservation are compared. The problems of the conventional small-signal model and the RF macro-model are addressed. Also, we investigate the bias dependence of small-signal parameters extracted using the proposed method. The  $I$ - $V$  characteristics constructed from the extracted transconductance and conductance are compared with the measured DC  $I$ - $V$  characteristics.

## 2 CONSTRUCTION OF CHARGE CONSERVING SMALL-SIGNAL EQUIVALENT CIRCUIT AND ITS PARAMETER EXTRACTION METHOD

We have proposed a simple and accurate parameter extraction method for a small-signal MOSFET model including the substrate-related parameters and a complete set of non-reciprocal capacitors [8]. This work uses a charge-conserving and physical small-signal equivalent circuit of the RF MOSFET and proposes an accurate parameter extraction approach by  $Y$ -parameter analysis from measured  $S$ -parameters.

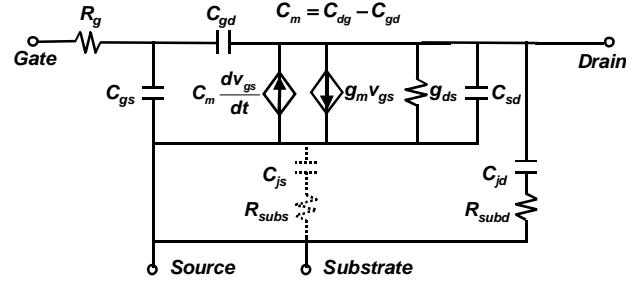


Figure 1: Small-signal equivalent circuit.

The small signal equivalent circuit of a three-terminal RF MOSFET model is shown in Fig. 1. Non-reciprocal capacitances and substrate-related parameters are included in the model. In three-terminal configuration,  $C_{js}$  and  $R_{subs}$  are excluded because the substrate is short-circuited to the source in most high-frequency application. Four intrinsic capacitances;  $C_{gs}$ ,  $C_{gd}$ ,  $C_{dg}$ , and  $C_{sd}$  are required for the three-terminal model. For simple circuit representation, the overlap capacitances are merged with the correspondent intrinsic capacitances.  $C_{gd}$  and  $C_{dg}$  are the two non-reciprocal capacitance components for a three-terminal model [5]-[7]. The capacitive effect of the drain on the gate is represented by  $C_{gd}$ , and the capacitive effect of the gate on the drain is represented by  $C_{dg}$ .  $C_m = C_{dg} - C_{gd}$  is a transcapacitance taking care of the different effect of the gate and the drain on each other in terms of charging currents [7].

Direct extraction using a linear regression approach is performed by  $Y$ -parameter analysis on the equivalent circuit of the MOSFET for high frequency operation. In our approach, an optimization process, which may have uncertainties in obtaining physical parameters, is not required. For operation frequency up to 10 GHz, by using the assumption that  $\omega^2 (C_{gs} + C_{gd})^2 R_g^2 \ll 1$ , the small-signal equivalent circuit shown in Fig. 1 can be analyzed in

terms of  $Y$ -parameters [8]. The validity of the assumption will be checked after each parameter is extracted.

All the components of the equivalent circuit are extracted by the  $Y$ -parameter analysis.  $g_m$  is obtained from the  $y$ -intercept of  $\text{Re}(Y_{21})$  versus  $\omega^2$  and  $g_{ds}$  is extracted from the  $y$ -intercept of  $\text{Re}(Y_{22})$  versus  $\omega^2$ , at the low frequency range.  $R_g$ ,  $C_{gd}$ ,  $C_{gs}$  and  $C_{dg}$  can be obtained by (1)–(4).

$$R_g = \text{Re}(Y_{11}) / (\text{Im}(Y_{11}))^2 \quad (1)$$

$$C_{gd} = -\text{Im}(Y_{12}) / \omega \quad (2)$$

$$C_{gs} = (\text{Im}(Y_{11}) + \text{Im}(Y_{12})) / \omega \quad (3)$$

$$C_{dg} = -\text{Im}(Y_{21}) / \omega - g_m R_g (C_{gs} + C_{gd}) \quad (4)$$

For the extraction of substrate components  $R_{subd}$  and  $C_{jd}$ ,  $Y_{sub}$  is first defined as follows:

$$\begin{aligned} Y_{sub} &= Y_{22} - g_{ds} - \omega^2 C_{gd} C_{dg} R_g - \omega^2 g_m R_g^2 C_{gd} (C_{gs} + C_{gd}) \\ &\quad - j\omega C_{sd} - j\omega C_{gd} - j\omega g_m R_g C_{gd} \\ &= \frac{\omega^2 C_{jd}^2 R_{subd}}{1 + \omega^2 C_{jd}^2 R_{subd}^2} + \frac{j\omega C_{jd}}{1 + \omega^2 C_{jd}^2 R_{subd}^2} \end{aligned} \quad (5)$$

$R_{subd}$  is obtained from the slope of the relationship for  $\omega^2/\text{Re}(Y_{sub})$  vs.  $\omega^2$  by (6).

$$\frac{\omega^2}{\text{Re}(Y_{sub})} = \omega^2 R_{subd} + \frac{1}{C_{jd}^2 R_{subd}} \quad (6)$$

$C_{jd}$  is obtained from the following.

$$C_{jd} = \left( \frac{\omega^2 R_{subd}}{\text{Re}(Y_{sub})} - \omega^2 R_{subd}^2 \right)^{-1/2} \quad (7)$$

Finally,  $C_{sd}$  is obtained from (8) as

$$\begin{aligned} C_{sd} &= \frac{\text{Im}(Y_{22})}{\omega} - C_{gd} - \frac{C_{jd}}{1 + \omega^2 C_{jd}^2 R_{subd}^2} - g_m R_g C_{gd} \\ &\quad + \omega^2 C_{gd} C_{dg} (C_{gd} + C_{gs}) R_g \end{aligned} \quad (8)$$

### 3 MODEL VERIFICATION

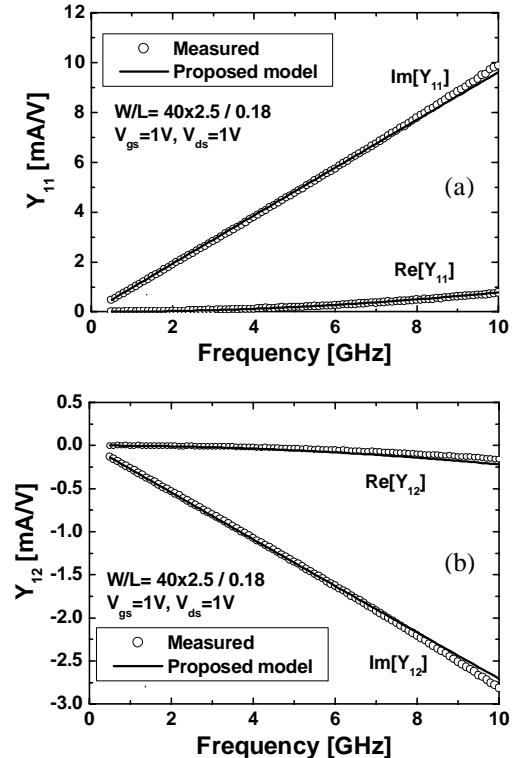
The proposed direct extraction method was applied to determine parameters of the test device, which is a multi-fingered n-MOSFET fabricated by 0.18  $\mu\text{m}$  technology.  $S$ -parameters were measured in the common source-substrate configuration using on-wafer RF probes and a HP 8510C

vector network analyzer. To remove on-wafer pad parasitics, a two-step deembedding was carried out by using the open and short deembedding structures. The parameters were extracted for an n-MOSFET with 100- $\mu\text{m}$  width having forty gate fingers.

$g_m$	48.5 mS
$g_{ds}$	3.2 mS
$R_g$	8.4 $\Omega$
$C_{gd}$	43.3 fF
$C_{gs}$	109.6 fF
$C_{dg}$	71.5 fF
$R_{subd}$	69.4 $\Omega$
$C_{jd}$	82.7 fF
$C_{sd}$	-16.8 fF

Table 1: Summary of extraction results.

All the small signal parameters were extracted at  $V_{gs} = 1$  V and  $V_{ds} = 1$  V. The extracted values of all parameters were summarized in Table 1. Due to the non-reciprocity,  $C_{dg}$  is larger than  $C_{gd}$  as it should be. For the extracted parameter values,  $\omega^2 (C_{gs} + C_{gd})^2 R_g^2$  is calculated to be 0.065 even at 10 GHz, which is much smaller than one. This confirms the validity of the assumption used for deriving (1)–(8).



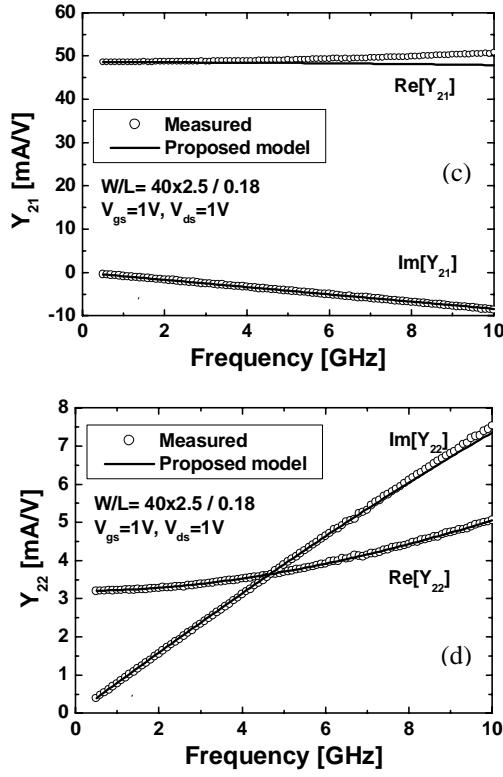


Figure 2: Modeled  $Y$ -parameters vs. measured  $Y$ -parameters: (a)  $Y_{11}$ , (b)  $Y_{12}$ , (c)  $Y_{21}$ , (d)  $Y_{22}$ .

In Fig. 2, the  $Y$ -parameters calculated with extracted parameters are compared with the measured data for  $V_{gs} = 1$  V and  $V_{ds} = 1$  V. It shows that the simulation result well matches the measurement without any optimization after direct extraction. The non-reciprocal capacitances  $C_{gd}$  and  $C_{dg}$  contribute to the imaginary parts of  $Y_{12}$  and  $Y_{21}$ . Excluding transcapacitance could result in a significant error on the imaginary part of  $Y_{21}$  at high frequencies. The substrate coupling significantly contributes to the output admittance  $Y_{22}$  at high frequencies. The total root-mean-square error between measured and modeled  $Y$ -parameters is only 1.8 %.

In Fig. 3, we compared the  $\text{Im}(Y_{12})$  and  $\text{Im}(Y_{21})$  from the conventional small-signal model [1] and the macro-model (Fig. 4) with the measured ones. The model parameters for these models were carefully extracted to best fit the measurement data. The small-signal model in [1] is very simple and doesn't have a complete set of charge conserving capacitances, which results in large discrepancy in  $\text{Im}(Y_{21})$ . We used the RF macro-model in Fig. 4. External  $C_{gsx}$  and  $C_{gdx}$  are added to describe the bias dependence of the overlap capacitance. These external capacitances also allow one to correct the inaccuracies of the intrinsic capacitances appearing for short-channel devices. However, with the reciprocal capacitance  $C_{gd}$ , we cannot simultaneously correct  $C_{gd}$  and  $C_{dg}$  (and thus,  $\text{Im}(Y_{12})$  and  $\text{Im}(Y_{21})$ ) as shown in Fig. 3. It also means that we cannot simultaneously fit both the feedforward gate-to-drain and

feedback drain-to-gate capacitances, which are very important for RF circuit design. Inaccuracy in capacitance can significantly affect the matching condition, gain, stability, noise figure, oscillation frequency, and so on. Fig. 2 demonstrates that the model with charge conserving capacitances can accurately fit both  $\text{Im}(Y_{12})$  and  $\text{Im}(Y_{21})$ .

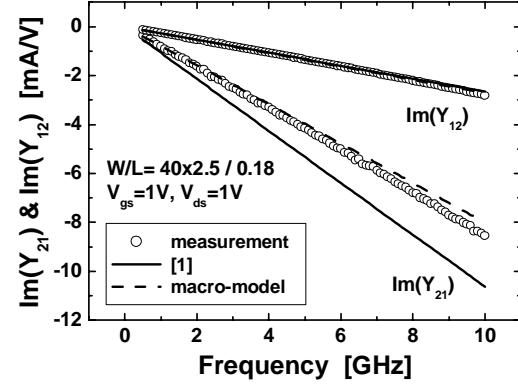


Figure 3:  $\text{Im}(Y_{12})$  and  $\text{Im}(Y_{21})$  from the models (a model of [1] and a macro-model) and the measurement.

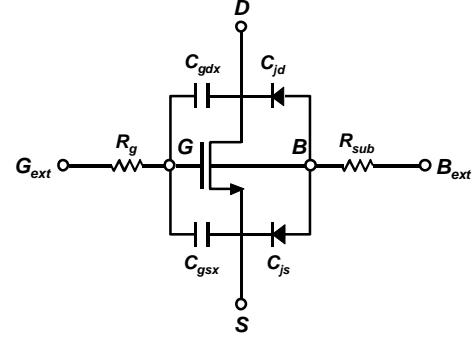
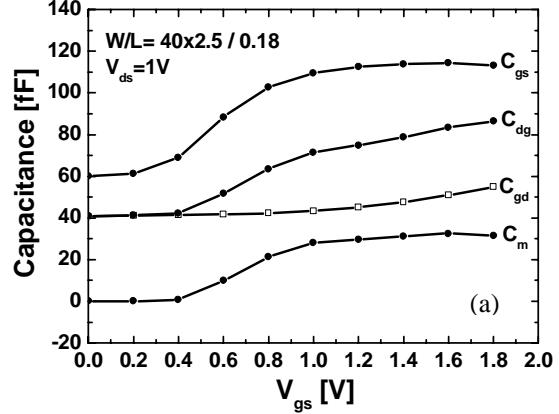


Figure 4: RF macro-model.

#### 4 BIAS DEPENDENCE OF THE EXTRACTED PARAMETERS



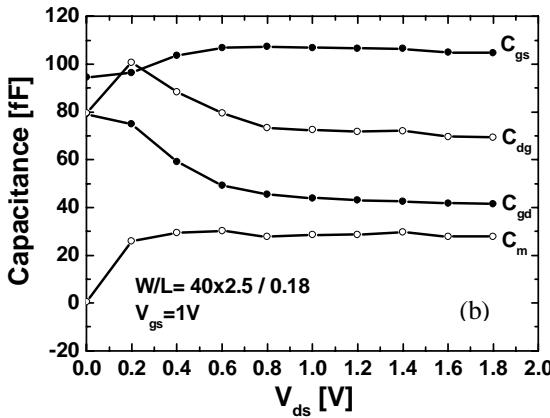


Figure 5: Bias dependence of capacitances: (a) gate bias dependence, (b) drain bias dependence.

Fig. 5 shows the bias dependence of the extracted capacitances; (a) for the gate bias dependence and (b) for the drain bias dependence. Note that the  $C$ - $V$  behavior is what we expect from MOSFET device physics and specifically that  $C_{dg}$  is larger than  $C_{gd}$ , demonstrating the necessity of considering transcapacitance of  $C_m$ . This consideration of charge conservation is important not only for the accuracy in circuit simulation but also for the compatibility with large signal  $Q$ - $V$  models [5]-[7].

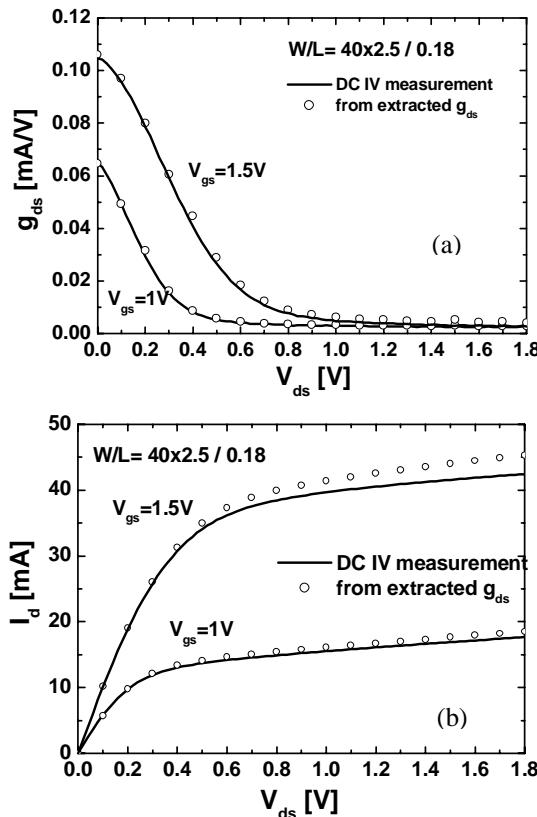


Figure 6: DC measurement vs. extracted results from  $S$ -parameters: (a)  $g_{ds}$  vs.  $V_{ds}$ , (b)  $I_d$  vs.  $V_{ds}$ .

The extracted  $g_{ds}$  values at  $V_{gs} = 1$  V and 1.5 V were plotted as a function of  $V_{ds}$  in Fig. 6(a) with the result from DC measurement while Fig. 6(b) shows  $I_d$ - $V_{ds}$  curves generated by integrating the extracted  $g_{ds}$  and the curves from DC measurement. Similar results were obtained for  $g_m$  vs.  $V_{gs}$  and  $I_d$  vs.  $V_{gs}$ . The results from  $S$ -parameter measurement at high-frequencies agree well with those from DC measurement. Therefore, one large-signal  $I$ - $V$  model is enough to be used for DC, low-frequency analog, as well as RF circuit simulation. Thus one should not worry about path independence in constructing large signal based on integration of measured small signal conductance data [7].

## 5 CONCLUSIONS

A charge conserving small signal equivalent circuit with very simple and accurate parameter extraction method for a three-terminal CMOS RF model was introduced. The parameters can be extracted directly from the real and imaginary parts of  $Y$ -parameters. Without any complex fitting or optimization step, the total root-mean-square error between the modeled and measured  $Y$ -parameters is only 1.8 %. The necessity of proper consideration for charge conservation is emphasized not only for accuracy in RF circuit simulation but also for compatibility with large signal  $Q$ - $V$  models. Lastly it is found that one accurate large-signal  $I$ - $V$  model is enough to be used for DC, low-frequency analog, as well as RF circuit simulation.

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