RF Applications of MOS Model 11

R. van Langevelde, A. J. Scholten, L. F. Tiemeijer, R. J. Havens, and D.B.M. Klaassen

Philips Research Laboratories
Prof. Holstlaan 4, 5656 AA Eindhoven, The Netherlands, Ronald.van.Langevelde@philips.com

ABSTRACT

RF-CMOS applications impose increasingly stringent requirements on compact models used in circuit simulation. In this paper several of these issues will be addressed together with a discussion of the state-of-the-art of compact modelling.

Keywords: RF-CMOS, compact modeling, noise, distortion, transit time, non-quasi-static, MOS Model 11

1 INTRODUCTION

As modern CMOS is rapidly progressing towards sub-100 nm dimensions, RF performance of MOS devices is improving strongly [1]–[4]. Therefore, CMOS has become a viable option for RF applications. To exploit the RF capabilities of CMOS, compact models for circuit simulation are required that describe all relevant quantities RF designers are interested in: not only currents and charges, but also noise figure, power gain, impedance levels, and harmonic distortion [5]–[7]. Here several of these issues will be addressed using Philips' new compact MOS model, MOS Model 11 (MM11).

MM11, successor to MM9 [8], has been developed in order to accurately describe the MOSFET currents as well as their higher-order derivatives (up to 3rd order) with respect to all terminal voltages. MM11 is based on a continuous description of the surface potential throughout all operating regimes, including the increasingly important moderate inversion regime. Compared to contemporary models such as BSIM4 [9] and MM9 [8], MM11 contains improved expressions for mobility reduction and velocity saturation. All relevant physical effects in today's MOSFETs, such as poly depletion, bias-dependent overlap capacitances, quantum-mechanical effects, and gate leakage current are included.

2 RF DISTORTION

Accurate modelling of harmonic distortion is important for the prediction of intermodulation during circuit simulation, e.g. for transceivers. Harmonic distortion measurements have been performed from 16 MHz to 1 GHz using an RF network analyzer (HP8753E; with an extension for 2^{nd} and 3^{rd} harmonic power levels) and were de-embedded up to the test-structure terminals [10]. Compact model parameters for MM11 are extracted from the DC current and its 1^{st}-order derivatives, and from low-frequency CV measurements. The compact model has been extended with parasitic resistances to describe polysilicon [11], [12] and bulk resistance [13] effects.

Measured and modelled results for a 0.35 μm n-MOS transistor as function of DC gate bias are shown in Fig. 1 for an intermediate frequency (f=16 MHz; left), and for an RF frequency (f=1 GHz; middle). At the right-hand side RF results for an 0.18 μm n-MOS transistor in 0.18 μm technology are shown. In all cases it is observed that MM11 (solid lines) gives an accurate description of HD1, HD2, and HD3. HD3 simulations using BSIM3v3 and MM9 are shown for reference. In contrast to what has been observed for bipolars [15], it was found that at f=1 GHz the description of distortion is still mainly determined by the DC drain current model of the MOSFET, while parasitic and intrinsic charges only contribute about -57 dBm to HD3. Accurate modelling results were also obtained for different drain biases, different technologies, and for PMOS (see e.g. [14]).

3 THERMAL NOISE

Accurate modelling of thermal noise is a prerequisite for the application of modern CMOS technologies to low-noise RF circuit design. In some publications [16], [17], it has been reported that thermal noise in submicron MOSFETs is increased considerably w.r.t. predictions based on long-channel thermal noise theory. Reported enhancements amount to more than a factor of 10 for n-channel devices as long as 0.7 μm, and are often attributed to hot-carrier effects. Contrary to this, we will show that drain current thermal noise of deep-submicron MOSFETs can be described accurately *without* invoking carrier heating or introducing any parameters (see also Ref. [18]). This is achieved by using the Klaassen-Prins formula [19], [20] combined with the appropriate equations for velocity saturation [18]. For the resulting expressions we refer to [8].

Drain current thermal noise is investigated at an intermediate frequency (248 MHz) where both low-frequen-

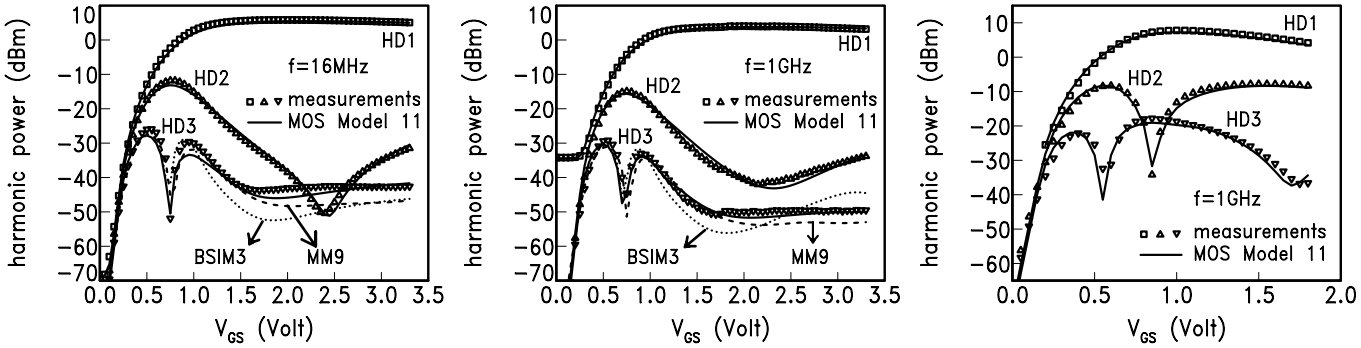

Figure 1: Distortion at $f = 16$ MHz (left), $f = 1$ GHz (middle and right) as a function of $V_{\rm GS}$ of a $16 \times 10/0.35$ μm n-channel device in 0.35 μm technology (left and middle) and $64 \times 3/0.18$ μm n-channel device in 0.18 μm technology (right). $V_{\rm DS} = 3.3$ V (left and middle); $V_{\rm DS} = 1.0$ V (right); $P_{\rm in} = -5$ dBm.

cy $1/f$ noise, and high-frequency induced gate noise can be neglected. We study the 50-Ohm noise figure F_{50} (i.e. noise figure at $50\,\Omega$ generator impedance), which is dominated by MOSFET drain current thermal noise. On-wafer noise measurements are performed using a conventional noise figure test set. A 50-Ω resistor is used to match the output impedance to the noise figure meter input. Besides the noise contribution of the MOSFET itself, all the device and interconnect parasitics, RF-probes, cables and bias-tees and the 50-Ω matching resistor have been characterized experimentally and included in the simulations.

In Fig. 2 F_{50} is plotted vs. $V_{\rm GS}$ for various channel lengths in 0.35 μm technology and for a 0.18 μm device in 0.18 μm technology. Our thermal noise model fits the data excellently. Note that all parameters used in the noise model are obtained from DC and low-frequency CV measurements; all experimental results are described accurately *without* introducing additional noise parameters, or invoking carrier heating or new physical phenomena. This implies that carrier heating effects are not large enough to enhance the thermal noise to a measurable extent. Possibilities why Refs. [16], [17] *do* find such a large enhancement are noise due to (i) weak valanche current [21] (ii) bulk resistance (included in our model) [22] or (iii) generation-recombination.

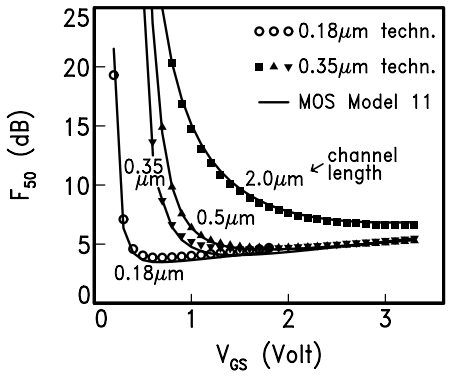

Figure 2: F_{50} vs. $V_{\rm GS}$ for various n-channels in 0.35 μm and 0.18 μm technology. ($V_{\rm DS} = V_{\rm DD}$, $W = 16 \times 10 \mu$m)

4 NON-QUASI-STATIC EFFECTS

To facilitate RF-CMOS circuit design, RF modelling tools should give an accurate description of quantities like power gain, input impedance and phase delay between drain current and gate voltage. To achieve this, not only parasitic resistances [11], [13], but also effects of finite channel transit times have to be taken into account. These so-called non-quasi-static (NQS) effects are included in various small-signal models (see e.g. [20], [23], [24]), which are, however, not suited for large-signal, transient and harmonic-balance simulations. An alternative model is the NQS extension of BSIM3 [25], which is computationally efficient, but is restricted to large-signal analysis. We follow the approach illustrated in Fig. 3, which is based on the idea of channel segmentation [20], [26], [27]. Advantages of this approach are that (i) it is physically sound, (ii) it can be used in all kinds of circuit analysis (DC, small-signal, transient, and noise analysis), and that (iii) all parameters are determined from DC- and low-frequency CV-measurements.

Experimental Method Using an HP8510 network analyzer, small-signal S-parameters [28] have been measured for various devices in ground-signal-ground configuration, fabricated in 0.18 μm CMOS technology. Measured S-parameters are converted into Y-parameters [28]

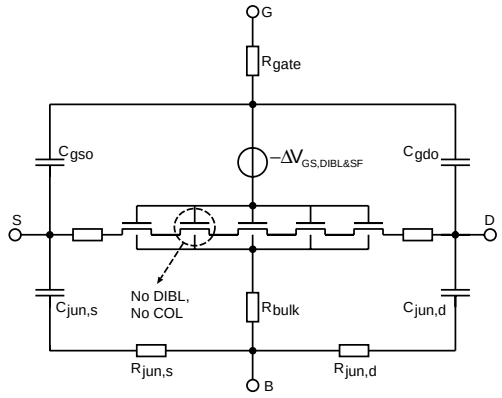

Figure 3: NQS model consisting of five MM11 segments.

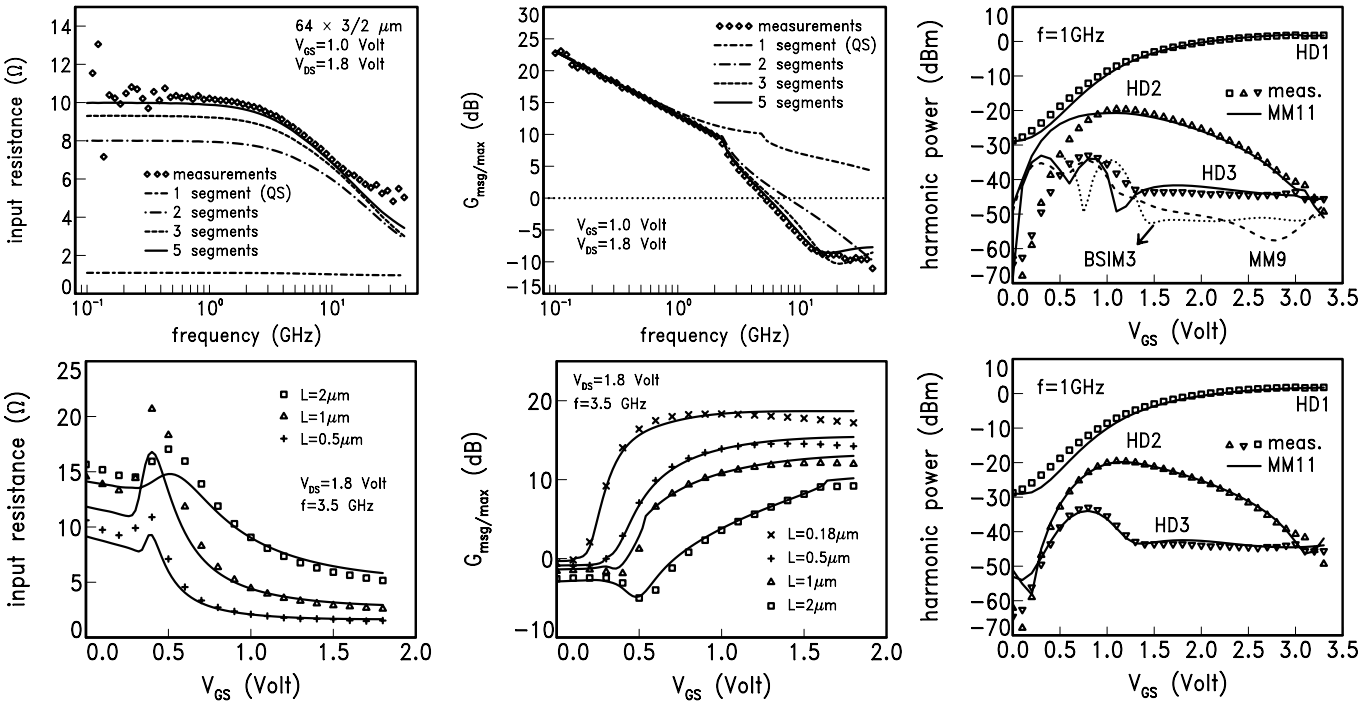

Figure 4: **Left/upper:** Symbols: input resistance versus frequency for a $64 \times 3/2$ μm n-channel in 0.18 μm technology. Lines are calculated with different number of channel segments. **Left/lower:** Symbols: input resistance at 3.5 GHz versus $V_{\rm GS}$ for a number of channel lengths. Gate width is 64×3 μm. Lines are calculated with a 5-segment NQS model. **Middle/upper:** Symbols: maximum stable/available power gain versus frequency for a $64 \times 3/2$ μm n-channel in 0.18 μm technology. Lines are calculated with different number of channel segments. **Middle/lower:** Symbols: maximum stable/available power gain at 3.5 GHz versus $V_{\rm GS}$ for a number of channel lengths. Gate width is 64×3 μm. Lines are calculated with a 5-segment NQS model based on MM11. **Right/upper:** First, second, and third harmonic distortion power levels of a $W/L = 160/2$ μm n-channel device in 0.35 μm technology. $V_{\rm DS} = 3.3$ V; $P_{\rm in} = -5$ dBm. **Right/lower:** Same measurements as in right/upper part. Solid line is calculated with a 10-segment NQS model based on MM11.

and de-embedded up to the test-structure terminals. From Y-parameters, relevant quantities such as input impedance and maximum stable/available power gain are calculated.

Input Resistance One of the key parameters for RF-CMOS designers is the input impedance. Here we consider $R_{\rm in} = {\rm Re}(1/Y_{11})$, the input impedance in case the output is ac-shortcircuited. This quantity is equal to zero for a QS model without parasitic resistances. In reality, however, it has a finite value (Fig. 4 left/upper part), which is partly due to parasitic resistances, but mainly due to the NQS effect. This is shown in the left/upper part of Fig. 4 by varying the number of channel segments, $N_{\rm seg}$, in our NQS model: by increasing $N_{\rm seg}$, simulations rapidly approach the measurements. We have found for linear (theoretically) and saturation regimes (empirically) that for frequencies well below $f_{\rm T}$:

$$R_{\rm in}(N_{\rm seg}) = R_{\rm in}^{\rm NQS} \cdot \left(1 - \frac{1}{N_{\rm seg}^2}\right) \qquad (1)$$

where $R_{\rm in}^{\rm NQS}$ is the NQS input impedance ($N_{\rm seg} \to \infty$). From Eq. (1) we see that with $N_{\rm seg} = 5$ the modelled $R_{\rm in}$ only deviates 4% from $R_{\rm in}^{\rm NQS}$. With $N_{\rm seg} = 5$ an accurate description is also obtained for $R_{\rm in}$ as function of $V_{\rm GS}$ for various channel lengths (Fig. 4 left/lower part).

Maximum Power Gain The maximum stable/available power gain [28] is defined as:

$$G_{\rm msg/max} = \begin{cases} \left|\frac{Y_{21}}{Y_{12}}\right| & \text{if } K < 1 \\ \left|\frac{Y_{21}}{Y_{12}}\right| \cdot \left(K - \sqrt{K^2 - 1}\right) & \text{otherwise} \end{cases} \qquad (2)$$

where K is the Rollett stability factor. The frequency at which $G_{\rm msg/max} = 1$ defines the maximum oscillation frequency $f_{\rm max}$. In the middle/upper part of Fig. 4, it is seen that a quasi-static model is not able to predict $f_{\rm max}$ for an $L = 2$ μm device. Using the NQS model, however, it is seen that the fit between model and data improves considerably when $N_{\rm seg}$ is raised to five. In general, the number of segments needed depends on channel length and operation frequency. For $N_{\rm seg}$ as low as 5, we see in the middle/lower part of Fig. 4 that $G_{\rm max}$ is modelled very well for a range of channel lengths $L < 2$ μm over the full gate bias range in saturation.

HF Distortion and NQS Effects In the right/upper part of Fig. 4, 1 GHz distortion data for a 2μm n-channel

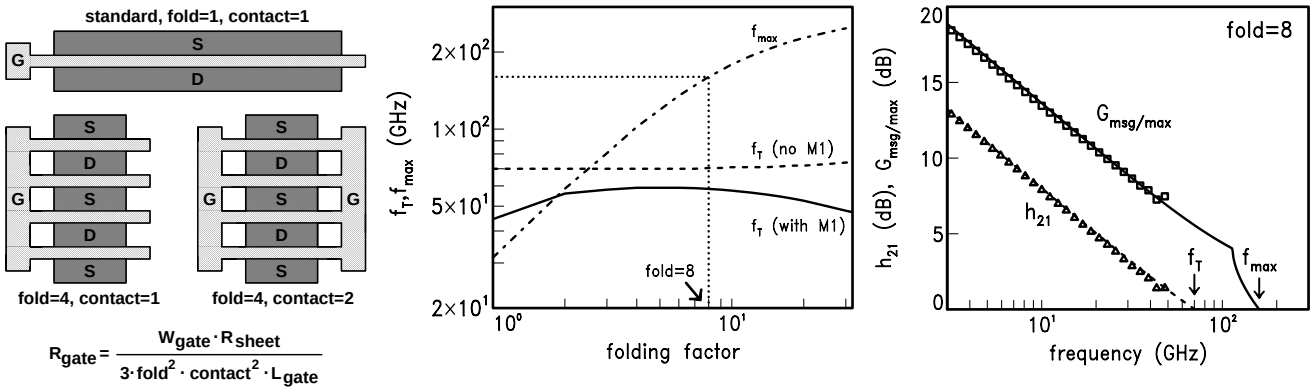

Figure 5: **Left:** Explanation of folding factor and gate resistance. **Middle:** Simulated f_T and f_{max} vs. folding factor. For f_T simulations are shown with and without the capacitance of the metal 1 (M1) stripes used to connect the gates fingers. **Right:** Measured (symbols) and simulated (lines) h_{21} and maximum stable/available power gain vs. frequency. All data are for a 32/0.18 μm n-channel device (contact = 2) in 0.18 μm technology with $V_{DS} = 1.8V$ and $V_{GS} = 1.0V$.

transistor are shown. At low values of gate bias the QS model no longer gives good results. In this bias region the harmonic frequency exceeds the cut-off frequency f_T and as a result the quasi-static approach is no longer valid. The right/lower part of Fig. 4 shows that the NQS-model with N_{seg}=10 gives accurate results over almost the whole bias region.

Layout optimization The gate resistance (Fig. 3 and Fig. 5; left) is one of the important elements determining the RF performance of a MOSFET. Having established the accuracy of our NQS model (Fig. 3), we used this model to optimize the RF performance of our devices by varying the layout (Fig. 5; left), yielding an optimal folding factor of 8 (Fig. 5; middle). Measurements on a device with this optimal folding factor of 8 are in agreement with the simulations (Fig. 5; right) and yield a record high f_{max} of 150 GHz for 0.18 μm CMOS technology ($\approx 2 \times f_T$) [4].

5 CONCLUSION

Various aspects of compact modelling for RF-CMOS have been addressed. First, we have shown that MOS Model 11 forms an excellent basis for RF-CMOS circuit design, because, in contrast to other contemporary compact models, it describes accurately the higher-order derivatives of the drain current, which results in an excellent description of third-order harmonic distortion. Moreover, we have shown that drain current thermal noise can be *predicted* with MOS Model 11: carrier heating effects or other additional physical effects need not be included to get a good description of noise data. Next, we have presented a simple yet effective method to turn a QS model into an NQS model by applying channel segmentation. Finally, we have demonstrated that our NQS model can be used in layout optimization of RF devices, yielding a record high f_{max} of 150 GHz for 0.18 μm CMOS technology.

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