Present Status and Future Direction of BSIM SOI Model for High-Performance/Low-Power/RF Application

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ABSTRACT

The recent progress of BSIM (Berkeley Short-channel IGFET Model) SPICE models extended for SOI transistors are reviewed. The models cover partially depleted (PD), fully depleted (FD) and dynamic depletion (FD) (automatically transition between PD and FD). The key concept of dynamic depletion will be discussed.

Keywords: SOI, compact model, fully depleted, partially depleted, history effect

1 INTRODUCTION

SOI technology have successfully penetrated into various applications including high-performance microprocessor [1], ultra-low power logic and RF system-on-chip applications [2]. Partially Depleted PD-SOI is the most popular form of SOI technology because its ease in manufacturability and compatibility with bulk CMOS processing. Ultra-thin film PD-SOI technology offers better short channel control over bulk technology [3]. Extremely high current drive devices with physical gate length down to 33nm were demonstrated recently for 0.10um generation high performance logic application (figure 1). In any case, almost all major IC manufacturing companies have SOI technology on their roadmap. The only question remains is whether SOI is inserted at 0.10μm or 0.07μm generation for those companies. It is worth notice that IBM has adopted SOI since 1998 with 0.22um generation.

SOI technology is particularly attractive for low Vdd low power because it's superior sub-threshold slope. This advantage is also true for both FD-SOI and PD-SOI In PD, due to beneficial gate-to-body capacitive coupling, body potential is raised as gate voltage increases provided that the junction capacitance is small enough [4]. Fig. 2 shows inverter delay less than 70ps at 0.5V supply achievable using state-of-the-art 0.13um CMOS. On the other hand, SOI devices show superior RF characteristics because of its low parasitics capacitance. Fmax up to 100GHz has been demonstrated (Fig. 3). These high Ft and Fmax values are very close to the best reported bipolar device. Along with high-Q capacitor and inductance, PD-SOI technology is the ideal platform for wireless system-on-chip application. The main obstacle, from my point of view, is to provide a good compact model for circuit designer so that the circuit behaviors at ultra-low supply voltage and high frequency characteristics are well predicted. In this aspect, the progress in compact model is well behind the technology advancement, especially in the fully depleted case.

2 CLASS OF SOI MODEL

SOI model can be classified into three categories : Partially Depleted (PD), Ideal Fully Depleted (FD) and Dynamic depleted (DD) (Table 1).

2.1 PD-SOI model

The latest BSIMPD2.2 [5,6] released by our group has been standardized by Compact Model Council (CMC) on Dec 9th, 2001. BSIMPD has been tested extensively in IBM and other companies. The current model covers almost all the major physics of PD-SOI including impact ionization current, gate-to-body tunneling current, ideal and non-ideal body contact, diffusion capacitance, trap-assisted tunneling diode, channel length dependent lateral bipolar and MOS-IV at very high Vbs. The gate-to-body tunneling current (Igb) is the latest added feature which is extremely important in PD-SOI. Igb can charge up the body and change the linear current characteristics (Fig. 4). Igb can also affect the history effect significantly (Fig. 5). The model framework of BSIMPD is 100% compatible with BSIM3 model. It makes it easier to adopt any additional formulation from the bulk model. Recent improvements in BSIM4 such as QM inversion charge thickness and RF formulation can be easily incorporated to BSIMPD model in near future. So far, there is no outstanding convergence problem in the SPICE3 implementation and others commercial SPICE simulators.

2.2 FD and DD model

The definition of fully depleted device varies between different companies and research group. However, from modeling point of view, as long as the device has any chance of getting full depletion in the simulation, a FD model is needed. Strictly speaking, a fully depleted model has to

handle transition from FD to PD because all SOI devices can operate at accumulation by applying a proper gate bias. However, it is not trivial to formulate a model that handle the FD-PD transition well [7]. Even if one can, the model will be very complicated to understand. It will be difficult to extract parameter and may be difficult to converge in large circuit simulation. In light of this, it is desired to divide fully depleted model into ideal FD and dynamic depletion (DD).

For devices with relatively low channel doping and the body is fully depleted at zero or even negative Vgs, the chance of getting partially depleted condition is very small. Then it is desirable to skip modeling the floating body. The model then contains only four nodes : gate, source, drain and backgate. The surface potential can be affected by both frontgate and backgate potential. Since there is no floating body, history effect is irrelevant. Though there is always some extent of history effect in all SOI devices, the error should be small enough to be neglected. Ideal FD model is very easy to formulate compared to PD. The junction IV and CV are not included in FD model. It then saves the computation time significantly. There is no need to make the FD model 100% compatible with bulk model because there is major difference in the bulk charge effect and threshold voltage calculation.

For devices only fully depleted at high gate bias, it may be necessary to use a model supporting dynamic depletion (DD). To precisely determine when to use ideal FD or DD models, we need a parameter that can describe the "degree" of full depletion. The key concept here is barrier lowering of the gated diode. Let suppose the body is fully depleted and we assign the body potential at SOI bottom to be Vbso. As one forces a constant current into the body region, the current has to leak through the source. If the current level is low, the frontgate and backgate coupling is strong enough to hold the potential inside the body. Then the device threshold voltage is not affected. As the current level increases, majority carrier starts to accumulate at the bottom and build up a finite potential. Then the "body potential" increases as show in Fig. 6. Therefore, the gate diode behaves like normal diode if Vbs is larger than Vbso. This phenomena is known as barrier lowering. Using the concept of barrier lowering, the appearance of kink in FD devices can be explained.

The Vbso at Vgs=0V can be used to measure the degree of full depletion. For example, if Vbso is –0.2V, it means that the device is PD at Vgs=0V because the reversed diode current or any thermal generation current can charge up the body to positive Vbs value. Another example, if Vbso is 0V, the device is just FD at Vgs=0V and very likely to be FD at turn on. Vbso can be measured experimentally or predicted by numerical device simulation. Fig. 7 illustrate how Vbso can be extracted from the subthreshold characteristics under different backgate biases. Vbso can be lowered by using negative backgate bias. By gradually reducing the backgate bias, the point where Vbso crossing zero can be detected from the transition between ideal subthreshold slope and a larger subthreshold slope.

As a rule of thumb, for Vbso > 0V, we suggest to use ideal FD model for simplicity, ease of extraction and robust circuit simulation. The penalty is the inability to predict history effect, kink effect and bipolar breakdown behavior. For Vbso < 0V, dynamic depletion model is preferred. Figure 8 shows the Id-Vd of a device under zero and –3V backgate bias. The appearance of kink indicates the need for dynamic depletion. For very negative Vbso (e.g., < -1V), it is very unlikely that the device can become fully depleted. Then PD-SOI model is recommended.

In bulk model, Vbs is defined as the potential of a neutral body. It is equivalent to say that the vertical electrical field at the body is zero. However, at full depletion, the body potential is coupled and therefore E-field is not zero. In order to handle the PD/FD transition, the model need to assign a body potential in any occasion. Then we need to convert the coupled body potential into a zero-field Vbs as shown in Fig. 9 and 10.

CONCLUSION

SOI technology has become the mainstream technology for high performance microprocessor and is emerging as a potential candidate for system-on-chip applications. Progress in compact modeling has been relatively slow comparing to the advances in technology development. Among the three types of SOI model, BSIMPD is well established. Meanwhile the ideal FD and DD models are work in progress. The key concepts in DD models are barrier lowering of gated diode and conversion of coupled body potential to zero-field Vbs.

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Table 1 : Three classes of SOI model

Model class	**Partially Depleted (PD) BSIMPD2.2**	**Ideal Fully Depleted (FD) BSIMFD2.1**	**Dynamic Depletion (DD) BSIMDD2.1**
Progress	Industrial quality, widely adopted in industry, Standardized by CMC on Dec 9th, 2001	Under continuous improvement	Under continuous improvement
Devices characteristics	Never get into full depletion	At least fully depleted at Vgs=0V	At least fully depleted at Vgs=Vdd
Number of nodes	G, D, S, B 4	G, D, S, E 4	G, D, S, B, E 5
Diode leakage & Gate-to-body tunneling current	Very critical	Not needed	Less critical Hard to formulate and calibrate
Diode capacitance & Body-to-Gate/Channel capacitance	Very critical	Not needed	Less critical Hard to formulate and calibrate
Simulation Time	Good	Faster	Slower
Convergency	Demonstrated	Even better	Not know yet
Compatibility with bulk model (BSIM3/BSIM4)	Essential	Not necessary	Essential

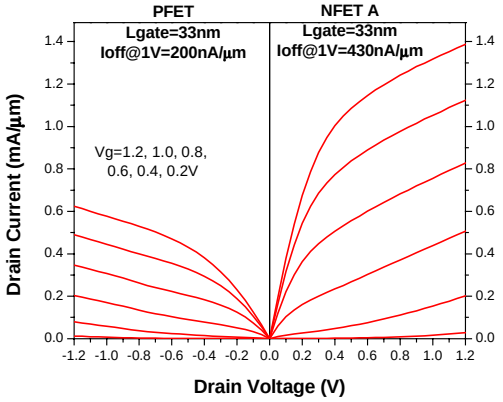

Fig. 1 Id-Vd of state-of-the-art 0.1um PD-SOI transistors showing very high current drive and excellent short channel control.

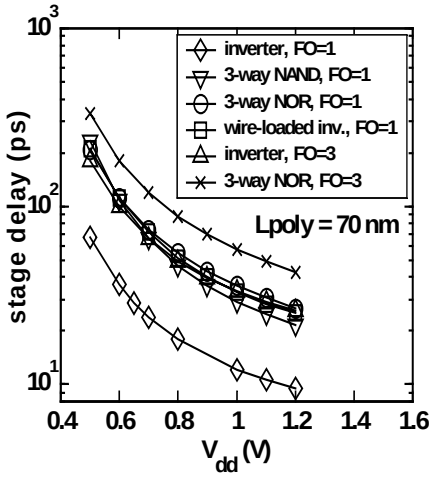

Fig. 2 Stage delay of stacked and non-stacked circuits with different loads in 0.13um SOI CMOS technology. The unloaded inverter delay at Vdd=0.5V is below 70ps.

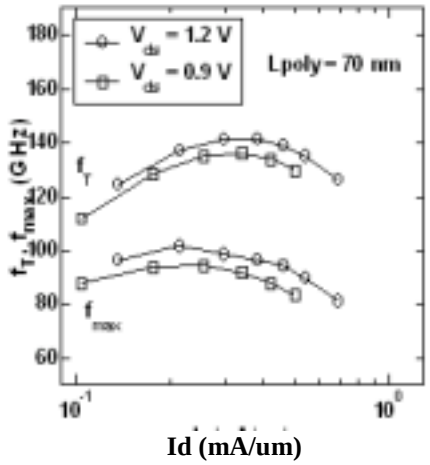

Fig. 3 Ft and Fmax of low-Vt NFET in 0.13um SOI CMOS technology. These Ft and Fmax values are comparable to high speed bipolar devices.

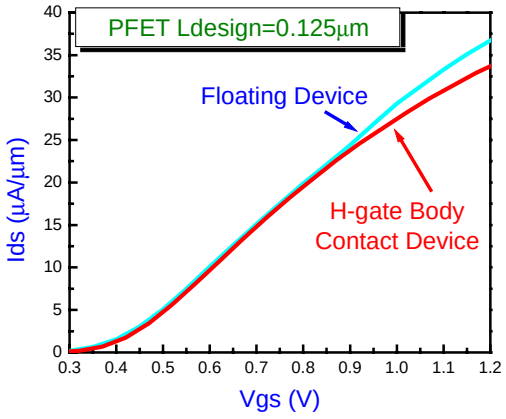

Fig. 4 Gate-to-body tunneling current (Igb) effect on floating body linear current.

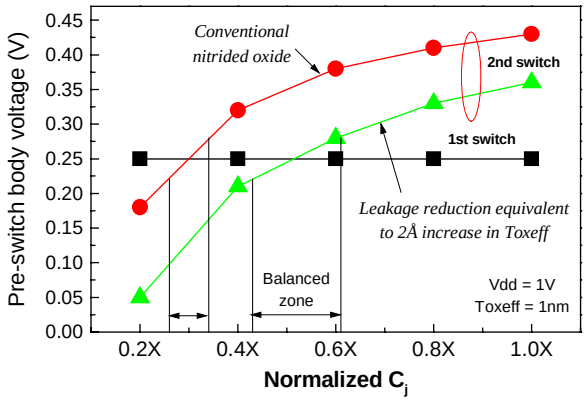

Fig. 5 Gate-to-body tunneling current (Igb) raises the pre-switch body voltage for the 2nd switch and therefore affects the history effect.

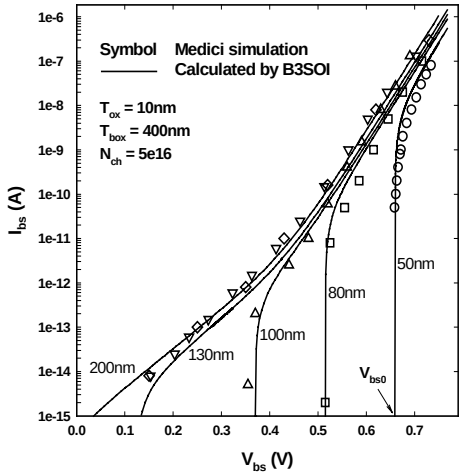

Fig. 6 Body-source diode characteristics under different extent of barrier lowering (Vbs0).

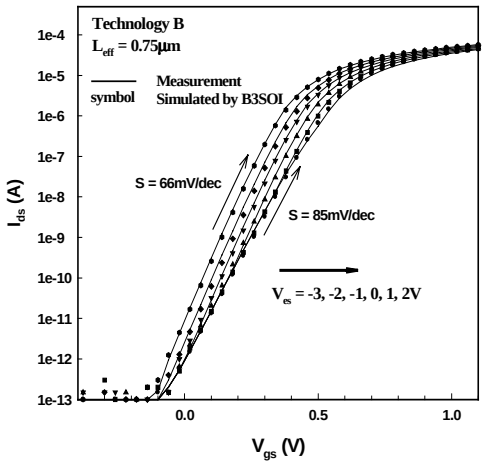

Fig. 7 Subthreshold slope characteristics with various backgate bias can be used for the extraction of barrier lowering (Vbso).

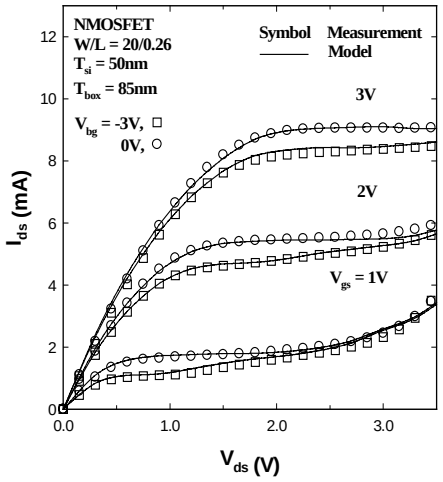

Fig. 8 Appearance of kink change with backgate bias for a device on the edge of full depletion.

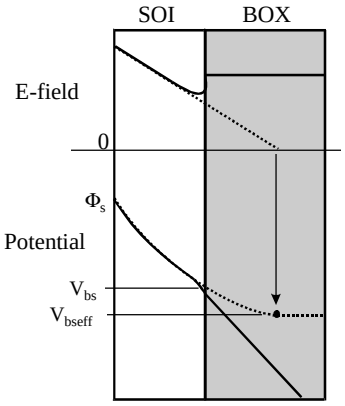

Fig. 9 In the case of full depletion, it is still possible to assign a zero-field "Vbs" for model formulation.

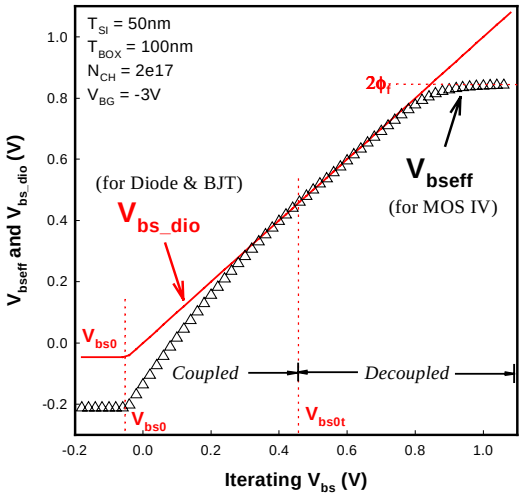

Fig. 10 Transition of body potential interpretation from decoupled to coupled operation.