RF MOSFET Noise Parameter Extraction and Modeling

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ABSTRACT

In this paper, a novel procedure for extracting the important noise sources in MOSFETs is reviewed. Examples of extracted noise sources as a function of frequency, bias and geometry are presented using devices from a 0.18 μm CMOS process and from RF noise measurements. A model for the channel noise current is proposed and comparisons to experimental data is presented.

I. INTRODUCTION

In addition to the high level of integration offered by CMOS process for digital circuit designs, MOSFETs have become attractive for RF applications due to the very high unity-gain frequencies of tens of GHz [1]. However, one of the challenges for the MOSFET-based RF circuit design is the prediction of the RF performance characteristics. In addition, when working at high frequencies, the noise generated within the device itself will play an increasingly important role in the overall system characteristics, especially for front-end receivers. Therefore understanding the RF and noise characteristics of MOSFETs is crucial for low noise, RF circuit designs.

In this paper, two main issues will be addressed. In the first part, the HF noise sources of MOSFETs extracted directly from the measured data are examined. Secondly, based on the noise knowledge obtained from measurements, a model for the channel noise current is proposed.

II. NOISE SOURCE EXTRACTION

A. Extraction Algorithm

The RF noise model of MOSFETs consists of two parts - a.c. lumped elements and noise sources. Fig. 1 shows a RF noise model of an intrinsic MOSFET that is suitable for high-frequency circuit applications. For the noise sources in fig. 1, $\overline{i_d^2}$ is the channel noise caused by the mobile carriers in the channel, $\overline{i_S^2}$ and $\overline{i_D^2}$ are the noise current sources caused by the source (R_S) and drain (R_D) resistances, $\overline{i_G^2}$ is the noise current source caused by the polysilicon gate resistance (R_G), and $\overline{i_{DB}^2}$, $\overline{i_{SB}^2}$, and $\overline{i_{DSB}^2}$ are the noise current source caused by the substrate resistance R_{DB}, R_{SB} and R_{DSB}, respectively. When transistors operate in the GHz range, the random potential fluctuations in the channel resulting in the channel noise will be coupled to the gate terminal through the gate oxide capacitance and cause the induced gate noise $\overline{i_g^2}$, which is usually correlated with the channel noise. The noise sources - $\overline{i_S^2}$, $\overline{i_D^2}$, $\overline{i_G^2}$ and $\overline{i_{DB}^2}$ are thermal noise with spectral density $4kT/R$ and will be determined as long as their corresponding resistance R is obtained through either DC or a.c. measurements. The noise sources that must be characterized are the channel noise $\overline{i_d^2}$, induced gate noise $\overline{i_g^2}$ and their correlation $\overline{i_g i_d^*}$.

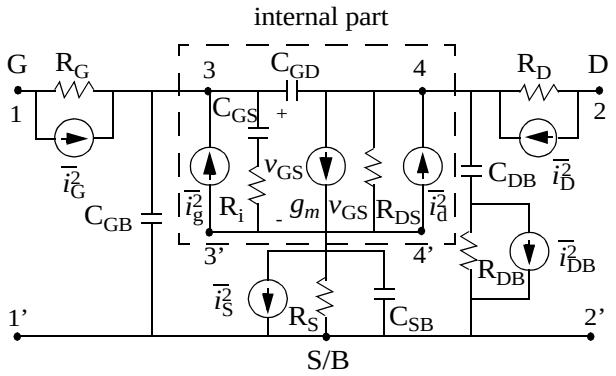

Fig. 1: The RF noise model of an intrinsic MOSFET that is suitable for high-frequency circuit applications.

The term $\overline{i_d^2}$ consists of the thermal noise (white noise) and the flicker noise. The flicker noise mainly affects the performance of the device at low frequencies and can be ignored at high frequencies, except for some RF circuits such as mixers or oscillators in which the low frequency noise will be up-converted to the frequencies around the carrier and deteriorate the phase noise and signal-to-noise ratio. If we divide the noise circuit into two parts - an internal part inside the dashed box and which consists of C_{GS}, C_{GD}, R_i, g_m, R_{DS}, $\overline{i_g^2}$ and $\overline{i_d^2}$, and an external part which includes all the components outside of the dashed box, after the devices and dummy structures, as described in [2], are fabricated, the induced gate noise, channel thermal noise and their correlation in MOSFETs can be extracted by using the following 15-step procedure.

1. Measure the scattering parameters $\boldsymbol{S_{DUT}}$, $\boldsymbol{S_{OPEN}}$, $\boldsymbol{S_{THRU1}}$ and $\boldsymbol{S_{THRU2}}$ of the device-under-test (DUT), OPEN, THRU1 and THRU2 dummy structures, respectively [2].
2. Measure the noise parameters, $NF_{min,DUT}$, $Y_{opt,DUT}$ and $R_{n,DUT}$ of the device-under-test (DUT).
3. Perform the parameter de-embedding to get the intrinsic scattering ($\boldsymbol{Y_{dev}}$) and noise parameters ($NF_{min,dev}$, $Y_{opt,dev}$ and $R_{n,dev}$) of the transistor [2].
4. Perform parameter extraction based on $\boldsymbol{Y_{dev}}$ and other measured data to get all the element values (e.g. g_m, C_{GS}, C_{GD},... etc.) in the RF noise model [3].
5. Calculate the correlation matrix $\boldsymbol{C_{Adev}}$ of the intrinsic transistor as defined in [4],[5].

6. Calculate the four-port admittance matrix $\boldsymbol{Y_{extr}}$ of the external part as defined in Fig. 1 by excluding all noise sources, C_{gs}, C_{gd}, g_m, R_{DS} and R_i, and partition $\boldsymbol{Y_{extr}}$ as

$$\boldsymbol{Y_{extr}} = \begin{bmatrix} \boldsymbol{Y_{ee}} & \boldsymbol{Y_{ei}} \\ \boldsymbol{Y_{ie}} & \boldsymbol{Y_{ii}} \end{bmatrix} \tag{1}$$

where $\boldsymbol{Y_{ee}}$, $\boldsymbol{Y_{ei}}$, $\boldsymbol{Y_{ie}}$ and $\boldsymbol{Y_{ii}}$ are 2×2 matrixes.

7. Calculate the two-port admittance $\boldsymbol{Y_{intr}}$ of the internal part shown in the RF transistor model.
8. Calculate the matrix $\boldsymbol{D}$ as follows [5]

$$\boldsymbol{D} = -\boldsymbol{Y_{ei}}(\boldsymbol{Y_{ii}} + \boldsymbol{Y_{intr}})^{-1}. \tag{2}$$

9. Convert the noise correlation matrix $\boldsymbol{C_{Adev}}$ to $\boldsymbol{C_{Ydev}}$ by

$$\boldsymbol{C_{Ydev}} = \boldsymbol{T_Y}\boldsymbol{C_{Adev}}\boldsymbol{T_Y}^{\dagger} \tag{3}$$

where the † in $\boldsymbol{T_Y}^{\dagger}$ denotes Hermitian conjugation and the transformation matrix $\boldsymbol{T_Y}$ is given by

$$\boldsymbol{T_Y} = \begin{bmatrix} -Y_{11,dev} & 1 \\ -Y_{21,dev} & 0 \end{bmatrix}. \tag{4}$$

10. Calculate the admittance noise correlation matrix $\boldsymbol{C_{Yextr}}$ of the external part by [6]

$$\boldsymbol{C_{Yextr}} = 2kT\Re(\boldsymbol{Y_{extr}}) \tag{5}$$

where $\Re(\,)$ denotes for the real part of the matrix elements, and partition $\boldsymbol{C_{Yextr}}$ as

$$\boldsymbol{C_{Yextr}} = \begin{bmatrix} \boldsymbol{C_{ee}} & \boldsymbol{C_{ei}} \\ \boldsymbol{C_{ie}} & \boldsymbol{C_{ii}} \end{bmatrix} \tag{6}$$

where $\boldsymbol{C_{ee}}$, $\boldsymbol{C_{ei}}$, $\boldsymbol{C_{ie}}$ and $\boldsymbol{C_{ii}}$ are 2×2 matrixes.

11. Calculate the admittance correlation matrix $\boldsymbol{C_{Yintr}}$ of the internal part in Fig. 1 by

$$\boldsymbol{C_{Yintr}} = \boldsymbol{D_i}(\boldsymbol{C_{Ydev}} - \boldsymbol{C_{ee}})\boldsymbol{D_i}^{\dagger} - \boldsymbol{C_{ie}}\boldsymbol{D_i}^{\dagger} - \boldsymbol{D_i}\boldsymbol{C_{ei}} - \boldsymbol{C_{ii}} \tag{7}$$

where $\boldsymbol{D_i} = \boldsymbol{D}^{-1}$.

12. Convert $\boldsymbol{Y_{intr}}$ to its chain representation $\boldsymbol{A_{intr}}$.
13. Convert $\boldsymbol{C_{Yintr}}$ to its chain matrix form $\boldsymbol{C_{Aintr}}$ by using

$$\boldsymbol{C_{Aintr}} = \boldsymbol{T_A}\boldsymbol{C_{Yintr}}\boldsymbol{T_A}^{\dagger}, \tag{8}$$

where $\boldsymbol{T_A}$ is given by

$$\boldsymbol{T_A} = \begin{bmatrix} 0 & A_{12,intr} \\ 1 & A_{22,intr} \end{bmatrix}. \tag{9}$$

14. Calculate the noise parameters, NF_{min}, Y_{opt} and R_n of the internal part in Fig. 1 from the noise correlation matrix $\boldsymbol{C_{Aintr}}$ by the equations (29a) - (29c) in [5].
15. Calculate the spectral density of the channel noise $\overline{i_d^2}$, induced gate noise $\overline{i_g^2}$ and their cross-correlation term $\overline{i_g i_d^*}$ by

$$\frac{\overline{|i_d|^2}}{\Delta f} = 4kTR_n\left|Y_{21,intr}\right|^2, \tag{10}$$

$$\frac{\overline{|i_g|^2}}{\Delta f} = 4kTR_n\left\{\left|Y_{opt}\right|^2 - \left|Y_{11,intr}\right|^2 + 2\Re[(Y_{11,intr} - Y_{cor})Y_{11,intr}^*]\right\} \quad \text{and} \tag{11}$$

$$\frac{\overline{i_g i_d^*}}{\Delta f} = 4kT(Y_{11,intr} - Y_{cor})R_n Y_{21,intr}^* \tag{12}$$

where Y_{cor} is given by

$$Y_{cor} = \frac{NF_{min} - 1}{2R_n} - Y_{opt}. \tag{13}$$

B. Experimental Results

Fig. 2 shows the extracted channel noise versus frequency characteristics for n-type MOSFETs with different channel lengths biased at V_{DS} = 1.0 V [13]. It is shown that the channel noise, in general, is frequency independent and increases when the channel length is decreased. This is because of the higher output conductance.

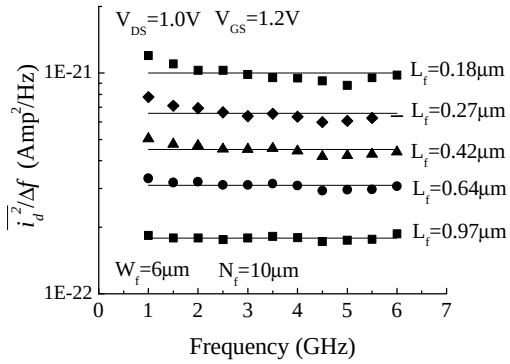

Fig. 2: Extracted channel noise ($\overline{i_d^2}/\Delta f$) versus frequency characteristics for n-type MOSFETs biased at V_{DS} = 1.0 V.

Figs. 3 and 4 show the extracted induced gate noise $\overline{i_g^2}$ and its correlation with the channel noise $\overline{i_g i_d^*}$ versus frequency characteristics for the n-type MOSFETs with channel width W = 10 × 6 μm (10 fingers of width 6 μm) and lengths L = 0.97 μm, 0.64 μm, 0.42 μm, 0.27 μm and 0.18 μm, respectively, biased at V_{DS} = 1.0 V and V_{GS} = 1.2 V [13]. It is shown that the induced gate noise and its correlation with the channel noise are proportional to f^2 and f, respectively where f is the operating frequency (solid lines in the figures). In addition, when channel length decreases, both the induced gate noise and the correlation term also decrease because of the decrease in the gate-to-source capacitance C_{GS}.

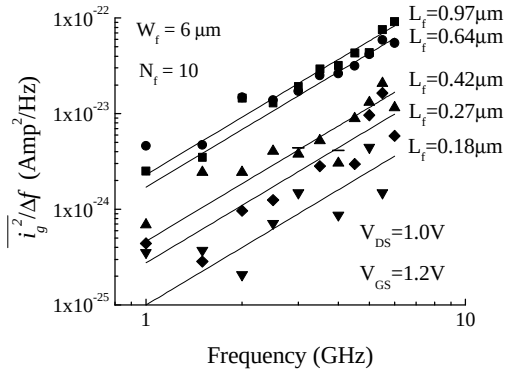

Fig. 3: Extracted induced gate noise ($\overline{i_g^2}$) versus frequency characteristics for n-type MOSFETs biased at V_{DS} = 1.0 V and V_{GS} = 1.2 V.

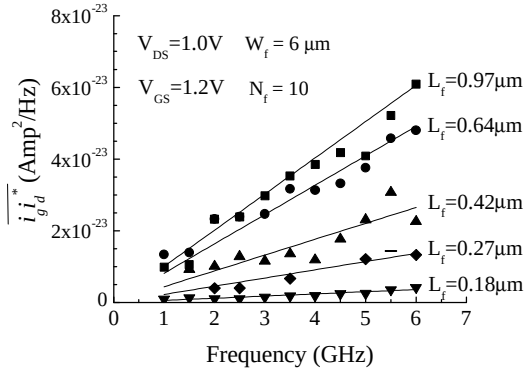

Fig. 4: The correlation between $\overline{i_g^2}$ and $\overline{i_d^2}$ ($\overline{i_g i_d^*}$) versus frequency characteristics for n-type MOSFETs biased at V_{DS} = 1.0 V and V_{GS} = 1.2 V.

III. CHANNEL NOISE MODEL

After having the direct targets for the channel noise from the direct extraction procedure using experimental data, the next step is to derive a physics-based analytical model. The approach used to calculate the channel noise is based on the model in which the channel of a MOSFET is divided into two regions - a gradual channel region of length $L_{elec} = L_{eff} - \Delta L$ (region I in fig. 5) and a velocity saturation region of length ΔL [7],[8] when the device is saturated, the normal operating mode for RFICs. In region I, the channel exhibits near ohmic conductivity and the gradual channel approximation holds. In region II, the carriers travel at their saturated velocity and the ohmic's law fails. Because the carriers in region II will not respond to any a.c. voltage fluctuation and produce zero noise current at the drain terminal, it is assumed that no noise current will be contributed from region II. Based on the noise model derived in [8] for region I, the spectral density of the channel noise can be obtained by

$$S_{i_d^2} = \frac{\overline{i_d^2}}{\Delta f} = \frac{4kT_o}{L_{elec}^2}\mu_{eff}(-Q_{inv}) + \delta\frac{4kT_oI_D}{L_{elec}^2E_{crit}^2}V_{DS} \qquad (14)$$

where k is Boltzmann's constant, T_o is the lattice temperature (K), μ_{eff} is the effective mobility, E_{crit} is the critical electrical field, I_D is the DC current, Q_{inv} is the inversion charge in the gradual channel region and V_{DS} is the voltage between the drain and the source terminals. If the device works in the saturation region, V_{DSsat} instead of V_{DS} will be used in equation (14). The second term in equation (14) is used to model the hot electron effect [10]. Because equation (14) is obtained based on the thermal noise theory which is only true in the gradual channel region, L_{elec} instead of L_{eff} will be used in equation (14) in order to model the channel length modulation (CLM) effects.

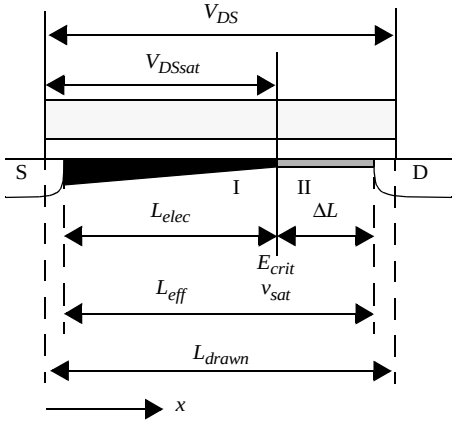

Fig. 5: Cross section of a MOSFET channel divided into a gradual channel region (I) and a velocity saturation region (II).

Fig. 6 shows the extracted (symbols) and simulated (lines) channel noise $\overline{i_d^2}$ versus V_{GS} characteristics for the n-type MOSFETs with channel width W = 10 × 6 μm and channel lengths L = 0.97 μm, 0.42 μm and 0.18 μm, respectively biased at V_{DS} = 1.5 V with δ = 0. The solid lines are obtained by using the L_{elec} in equation (14) and the dashed lines are obtained using L_{eff}. It seems that the hot electron effect does not have strong impact on the channel noise [9]. In addition, it is shown that the CLM effect begins to have some impact on the channel noise when the channel length of the device is smaller than 0.5 μm and the exclusion of the CLM effect will predict lower channel noise.

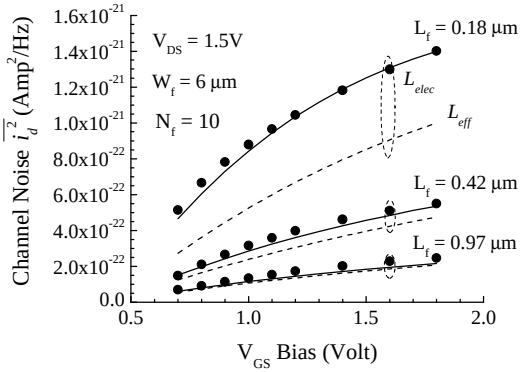

Fig. 6: Measured (symbols) and simulated (lines) channel noise $\overline{i_d^2}$ versus gate bias V_{GS} characteristics of n-type MOSFETs.

For the V_{DS} dependence of the channel noise, fig. 7 shows extracted (symbols) and simulated (lines) channel noise versus V_{DS} characteristics for the n-type MOSFETs with channel width W = 10×6 μm and channel lengths L = 0.97 μm, 0.42

μm and 0.18 μm, respectively biased at V_{GS} = 1.0 V with δ = 0. The solid lines are obtained using L_{elec} in equation (14) and the dashed lines are obtained using L_{eff} in the noise calculation. It is shown that the calculated channel noise using L_{eff} predicts lower channel noise and cannot mimic the increasing trend of the extracted channel noise caused by the CLM effect for the deep sub-micron devices.

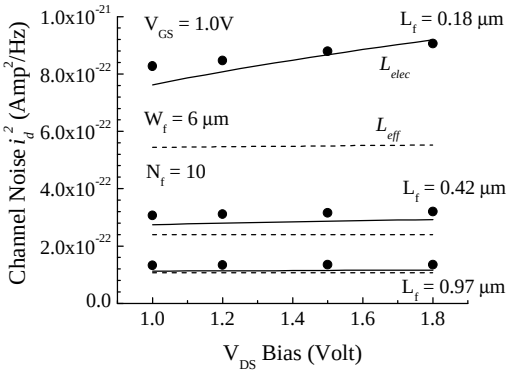

Fig. 7: Measured (symbols) and simulated (lines) channel noise $\overline{i_d^2}$ versus drain bias V_{DS} characteristics of n-type MOSFETs.

Sometimes, the spectral density of the channel noise $\overline{i_d^2}$ will be expressed by

$$S_{i_d^2} = \gamma \cdot 4kT_o g_{dso} \tag{15}$$

where g_{dso} is the output conductance at zero drain bias (i.e. V_{DS} = 0) [10]. For long-channel devices, the value of γ is between 1 (in the linear region with V_{DS} = 0) and 2/3 (in the saturation region) [10],[11]. However, for short-channel devices, the value of γ will become greater than 2/3 in saturation [12] and this is caused mainly by the CLM effect. Fig. 8 shows the measured (symbols) and simulated (lines) γ versus gate bias V_{GS} characteristics of an n-type MOSFET with channel length L = 0.18 μm and width W = 10 × 6 μm biased at V_{DS} = 1.5 V with δ = 0 and the noise contributed from the velocity saturation region.

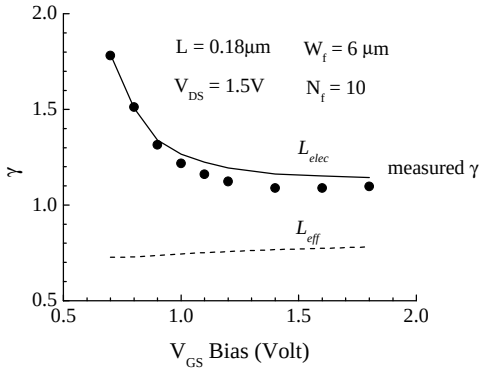

Fig. 8: Measured (symbols) and simulated (lines) γ versus gate bias V_{GS} characteristics of n-type MOSFETs.

It is shown that for the deep-submicron MOSFETs, the γ value will be increased from 2/3 to 1.2 or 1.8 (depending on the V_{GS} bias) when the channel length is reduced. In addition, at a fixed V_{DS} bias, the γ value will be decreased when the V_{GS} value is increased [9]. However, if the L_{eff} is used in the calculation of channel noise (dashed line in fig. 8), the γ factor increases towards to unity when V_{GS} is increased which is the opposite trend of the extracted channel noise.

IV. CONCLUSION

A general procedure to directly extract the induced gate noise, channel thermal noise and their correlation in MOSFETs from on-wafer scattering and noise measurements has been presented in detail. In addition, a physics-based channel noise model has been presented and verified. It is found that the channel length modulation (CLM) effect begins to have impact on the devices with channel length smaller than 0.5 μm. On the other hand, the noise contributions from the velocity saturation region and from the hot electron effect seem negligible in the channel noise modeling of deep sub-micron MOSFETs.

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