# Standardization and Validation of Compact Models

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## ABSTRACT

The idea of standardizing compact (SPICE-like) models has recently gained momentum in the semiconductor industry. However, since compact model equations reside in software, the concept of standardization is difficult. Several key issues must be addressed, such as accuracy, testing, availability, version control, verification and validation. Most compact models were developed without considering such issues and require productization for the compact model to be useful to the industry. The 1998 SIA Roadmap identified productization as a key issue for 100nm node [1].

With these issues in mind, a group of companies formed the Compact Model Council (CMC), chartered specifically to standardize compact model formulations. The CMC currently has 23 member companies (Table 1), including software vendors and semiconductor suppliers. The current standardization efforts include models for MOSFET (bulk), SOI MOSFET, and Si/SiGe BJT technologies.

## 1 BACKGROUND

Compact models were and continue to be developed in a number of ways, including university research, internal company research and development, and government funded research. Each group had a target in mind when the development started, and most of the models are applicable to the specific task at hand. However, for a compact model to be standardized, the focus must be extended to the entire semiconductor industry. The first requirement is to determine the current and short-term needs of the industry. Next, an appraisal of the existing compact models is required to determine the best candidate for standardization. Finally, the productization of the compact model chosen must occur for the standard compact model to be useful to the industry.

SEMATECH originally recognized in 1995 that productization of new compact models was the biggest challenge in their deployment. Several companies decided that a new group must be formed to address the need for compact model productization. The group formed was the CMC. The group found a home at the Electronics Industry Alliance (EIA) and began working to promote standardization of compact models in December 1995. The current CMC membership includes most of the largest semiconductor producers in the industry along with several EDA vendor companies. A membership fee is paid annually which funds the productization efforts and covers the administrative costs of the GEIA (the sector of the EIA where the CMC resides). The CMC does not fund any research, only the productization of compact models chosen to go through the standardization process.

| Compact Model Council Membership for 2001 | |
|---|---|
| Advanced Micro Devices | Agilent |
| Agere | Analog Devices |
| Atmel Wireless and µC | Avant! |
| Broadcom | Cadence |
| Circuit Semantics | Compaq |
| Conexant | Hitachi |
| IBM | Infineon |
| Intel | Intersil |
| Mentor Graphics | Motorola |
| NEC | Philips |
| SGS-Thomson | Texas Instruments |
| TSMC | |

Table 1: Compact Model Council members.

## 2 STANDARDIZATION PROCESS

What is the definition of a standard? Standards are documented agreements containing technical specifications or other precise criteria to be used consistently as rules, guidelines, or definitions of characteristics to ensure that materials, products, processes and services are fit for their purpose [2]. For compact models, a standardization process must be defined. The CMC reached consensus among its members on the process used for compact models standardization: 1) define the scope of the compact model, 2) define a method for verification of performance of the compact model, 3) document the results of the compact model performance testing, 4) make sure that the compact model is widely available for use by all companies, 5) employ revision control for the standard.

### 2.1 Scope of the model

Before choosing a standard compact model, the scope of the model must be defined. The CMC's first standardization effort, starting in 1995, was for the MOSFET technologies, focusing on the current production node and the next generation. The CMC determined that the business needs of its members were best served by standardizing a MOSFET model first, as it would have the biggest impact on the

industry. Several general characteristics were required for a candidate to be considered (Table 2).

| | |
|---|---|
| Public domain source code | Complete documentation |
| C language source code | Results on qualitative tests |
| Model support structure | Results on quantitative tests |
| Documented Parameter Extraction Methodology | Scalable for W and L |

Table 2: General model characteristics.

For the bipolar technology effort, the additional requirement of solver source code was added and scalability was dropped as a requirement. The C language source code requirement was also relaxed since most of the candidates had their origins in FORTRAN. These general model characteristics were not considered technical issues, however, in order for a compact model to be useful, these characteristics had to be addressed. The technical aspects of the candidates are discussed in the next section.

## 2.2 Qualitative and Quantitative testing

In order to compare compact models and their capabilities, a set of tests needed to be developed for each technology standard. Published information on compact models very rarely highlighted the completeness of a compact model and usually listed the effects and features the compact model contained without any mention of verification of the model performance. To address this need, the CMC and the group that evolved into the CMC (the Compact Model Workshop hosted by SEMATECH) chose several tests that would be performed on the model candidates to show the "goodness" of the model. The model should be accurate to the measured device behavior and should also be well behaved mathematically.

Compact models normally contain a set of equations with parameters that can be adjusted to properly model the technology being used. These parameters will determine the quantitative ability of the compact model. The behavior of the model equations will determine the qualitative behavior of the model. The tests chosen by the CMC for MOSFET models are listed below. For more information on the tests, please refer to the draft IEEE Recommended Practice P1485 located at the CMC Website: http://www.eigroup.org/CMC/

| MOSFET Qualitative and Quantitative Tests |
|---|
| Triode to saturation (TS) characteristics $I_d$ and $g_o$ |
| Threshold (TH) characteristics $I_d$ and $g_m$ |
| Subthreshold (ST) characteristics, $\log(I_d)$ and $g_m$ |
| Tsvidis/Suyama Tests 1-6 [3] |
| $I_{sat}$ and $V_{diode}$ over T and $V_{sb}$ for short and long devices where: $V_{diode}=V_{db}=V_{gb}$ and $I_d=0.1\mu A \times (W_d/L_d)$ |
| $I_{sat} \times L_m$ and $V_{diode}$ over $L_m$ |
| $I_{sat}/W_m$ and $V_{diode}$ over $W_m$ |
| Fine grid tests for $g_m$ and $g_o$ ($V_{gb}$ and $V_{db}$) - 3 tests |
| $\log(g_o)$ over $I_d$ |
| Gummel tests - 3 tests |
| Capacitance fine grid tests - 2 tests |

Table 3: MOSFET qualitative and quantitative Tests.

For the bipolar effort, a different set of tests was developed.

| Bipolar Qualitative and Quantitative Tests | |
|---|---|
| CV Tests | CJE vs. VBE<br>CJC vs. VBC<br>CJS VC VSC |
| AC Tests (S-Parameters De-embedded) | Real(Y) vs. Frequency<br>Imag(Y) vs. Frequency<br>Mag(Y) vs. Frequency<br>Phase(Y) vs. Frequency<br>$F_t$ vs. IC<br>$F_{max}$ vs. IC |
| Forward Gummel | IB vs. VBE<br>IC vs. VBE<br>IS vs. VBE<br>Temp vs. VBE<br>IC/IB vs. log(IC)<br>IC/(IB+IS) vs. log(IC)<br>(dIC/dVBE)/IC vs. VBE |
| Reverse Gummel | IB vs. VBC<br>IE vs. VBC<br>IS vs. VBC<br>Temp vs. VBC<br>IE/IB vs. log(IE)<br>IE/(IB+IS) vs. log(IE) |
| Forward Output (VBE) | IB vs. VCE<br>IC vs. VCE<br>IS vs. VCE<br>Temp vs. VCE<br>IC/IB vs. VCE<br>IC/(IB+IS) vs. VCE<br>IC/(dIC/dVCE) vs. VCE |
| Reverse Output (VBC) | IB vs. VEC<br>IE vs. VEC<br>IS vs. VEC<br>Temp vs. VEC<br>IE/IB vs. VEC<br>IE/(IB+IS) vs. VEC |
| Forward Output (IB) | IC vs. VCE<br>IS vs. VCE<br>VBE vs. VCE<br>Temp vs. VCE<br>IC/IB vs. VCE<br>IC/(IB+IS) vs. VCE<br>IC/(dIC/dVCE) vs. VCE |

Table 4: Bipolar qualitative and quantitative tests.

Note that there is no mention of required fit error percentage in these tests. Simply looking at the overall RMS error does not guarantee that a given parameter set actually characterizes the technology properly. The data taken for modeling is only a snapshot of the technology. Statistical methodologies must be employed to accurately model a technology.

For the current SOI standardization effort, all of the MOSFET tests were used as well as some additional SOI specific tests that are in the process of being documented.

These tests allowed CMC member companies to technically compare multiple models and determine which candidates performed well and which candidates performed poorly. To make sure that the model parameters were extracted correctly, the model developer was requested to extract the model parameter set for a given technology. This helped ensure that the results from the extraction were the best possible for the given technology.

## 2.3 Documentation of results

The results of the testing were reported to the CMC during its quarterly meetings. The results showed the strengths and weaknesses of the compact model candidates, and contributed to the consensus adoption of the CMC's standard models. In situations where candidates were considered to have performed equally, other considerations were taken into account. This occurred in 1995 during the evaluation of the MOSFET model candidates. Both candidates were considered to be technically comparable, however, the issue of public domain source code became the deciding factor in choosing BSIM3 [4] as the first MOSFET model to go through the standardization process.

## 2.4 Availability

To properly evaluate a compact model, a circuit simulator must have the compact model installed. This may sound like a trivial task, however, EDA vendors spend several people-months installing, evaluating, and updating compact models in their software tools. The CMC encouraged the EDA vendors to join so that the vendors would have inputs directly into the standardization process. Not only would the EDA vendors have a direct input to the model developers, but they also could share their best practices for software robustness with the model developers. During the standardization process, several errors in limiting functions, parameter boundary conditions, and other software specific corrections could be relayed to the model developers and incorporated into the code. This would make the standard compact model code much more robust and easier to implement in the future.

## 2.5 Revisions and updates

Once a candidate is chosen for standardization, the CMC begins productization of the compact model. Productization of a compact model requires that the compact model be transformed into a viable product that can be used in the industry. Changes would include model source code robustness, bug fixes, improved documentation, correction of numerical errors or problems, inclusion of more accurate portrayal of physical phenomenon, and software management procedures. These changes require accurate documentation so that the status of the standard compact model source code is well defined.

A standard compact model should contain the best practices used in the industry for modeling as well as for software management. These best practices are incorporated into the standard through the CMC member companies. For example, the BSIM3 compact model has had several revisions based upon recommended changes from CMC members, including parameter limiting functions (Avant!, Agilent, Mentor Graphics), improved mobility and substrate current modeling (Analog Devices), more accurate capacitance modeling (Infineon, SGS-Thompson, IBM), improved thermal noise modeling (Texas Instruments), and improved parasitic handling (IBM). These changes had to be differentiated from the original source code by adopting a revision and update scheme.

The CMC helped the BSIM development team [5] at the University of California at Berkeley establish a model code revision scheme that enabled organized, timely releases of bug fix versions as well as allowed for major revisions, such as adding new features or enhancements to existing features. The EDA vendors also provided a preferred schedule for the frequency of releases based upon their own release cycle. This ensured the CMC member companies had a timely installation of the standard model code for evaluation.

# 3 VALIDATION

Validation of compact models is done in stages. The EDA vendor is usually responsible for the first stage, installation of the compact model in the tool. The second stage, required due to the nature of compact models, is the responsibility of the model parameter set provider. This stage entails checking the model parameter sets for stability and a reliable simulation result. In the third, and final stage, circuit-level simulations are compared to measured data, providing the true validation of any compact model.

## 3.1 Installation

Each EDA vendor has their own requirements for validation of installation of compact models. The CMC recommends that validation of compact model installation be performed using the qualitative tests for the given technology (Section 2.2). The results should be verified with the simulator/solver that is provided by the model developer. A wide range of biases, device sizes, and parameter ranges should be checked. Any inaccuracies that are not acceptable should be traced to their point of origin. If the problem is with the model code itself, the problem

should be reported to the model developer with a suggested solution if one has been determined.

New model installations in proprietary simulation tools at Texas Instruments undergo similar testing. In fact, the model solver source code provided with the new model is used extensively to validate installation. This is particularly important for documenting the matrix stamp that defines the model's equivalent circuit representation. For example, with BSIM3, BSIM4 [6], and BSIMPD [7], Berkeley SPICE3 was the model solver source code used to verify implementation in both simulation and model extraction tools.

## 3.2 Model parameter quality

Parameter sets are notorious for causing simulation problems. Once a parameter set is created (fitted to measured data), the model's performance should be tested over a wide range of sizes, temperatures, and terminal biases (voltages and currents). Anomalies to look for are negative conductance, spikes, and other non-physical behavior. Most semiconductor device characteristics are smooth and continuous, however, compact models are based upon simplifying assumptions that may cause the model's behavior to be less than desirable. This kind of behavior can cause convergence issues with simulations.

At Texas Instruments, a proprietary tool was developed and is used extensively for parameter set testing. This tool has also been used to identify undesirable mathematical behavior, which has aided model improvements coordinated by the CMC.

## 3.3 Circuit-level performance

The final validation for a compact model is derived from comparisons of circuit simulations and measurements, with proper accounting for process variation and the affects of circuit parasitics, e.g., interconnect and package. Full circuit simulation is the also the best way to test the convergence properties of a compact model. This is particularly true for advanced models that comprehensively account for all physical mechanisms important in leading-edge technologies.

At Texas Instruments, the circuit designers that depend upon the simulation ultimately determine whether or not a compact model is useful.

# 4 SUMMARY

This paper describes an organization of compact modeling experts from leading semiconductor and EDA companies that manage the promotion of compact modeling best practices. These currently include BSIM3 and BSIM4 for bulk CMOS and BSIMPD for partially-depleted SOI. The paper documents the process that the CMC uses to create standard compact models and contains examples of what is required for a compact model to be standardized. Texas Instruments fully supports the efforts of the CMC and considers it to be a valuable resource for new model productization.

# REFERENCES


[1] SIA Roadmap update, Tables 62 and 63, 1998.

[2] Unknown, "Introduction to ISO, What are Standards?," January, 1999.

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[4] W. Liu, C. Hu, X. Jin, J. Chen, M. Jeng, Z. Liu, Y. Cheng, K. Chen, M. Chan, K. Hui, J. Huang, R. Tu, P. Ko, "BSIM3v3.2.2 MOSFET Model User's Manual," 1999.

[5] http://www-device.eecs.berkeley.edu/~bsim3/.

[6] W. Liu, X. Jin, K. M. Cao, C. Hu, "BSIM4.0.0 MOSFET Model User's Manual," 2000.

[7] BSIM Research Group, "BSIMPD2.1 MOSFET Model User's Manual," 1999.



* Britt Brooks is also the Compact Model Council Chairperson.