Extraction of Coupled RLC Network from Multi-level Interconnects for Full Chip Simulation

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ABSTRACT

In this paper, an approach is proposed for extracting coupled RLC network from multi-level interconnects. The proposed approach starts with a step of partitioning the layout of the full-chip under consideration into several sub-layouts, followed by steps of fracturing the partitioned layout and transforming into the three-dimensional structure. The layout is then classified into three species of segments, i.e. electrical node segments, resistive segments, capacitive segments, in order to generate a coupled RLC network from the layout data. These segments are employed for specifying the simulation domain and the boundary condition. Finally, the parasitics are calculated by a finite element method. A sampler circuit, which has 24 transistors for a 3.3V CMOS technology with 0.3μm feature size, was examined for the application of our approach. In this work, the number of nodes for FEM calculation was 68,115 with 375,624 tetrahedrons, and the required CPU time was approximately one hour on ULTRA SPARC 10 workstation.

Keywords: Interconnect, RLC network, 3D FEM, Circuit Simulation.

1. INTRODUCTION

Multi-levels of interconnections improve propagation delay significantly and are essential for high performance VLSI [1]. However, multi-level scheme makes the shape of interconnection in VLSI circuit geometrically complex, and each parasitic element of interconnections represents the electrical behavior of a complex three-dimensional object. Therefore, the characterization of parasitic elements and the analysis of electrical properties for such complex interconnection structure become essential for system synthesis and optimization. However, due to the complexity of geometry, the computation for parasitics in interconnects is hard to be understood by analytical method.

Many numerical methods have been applied to extract the electrical parameters of the interconnect structure. However, these electrical parameters are generally modeled as lumped RC networks. As the speed of integrated circuits increases, it is highly desirable to include the distributed nature of interconnects in order to ensure accurate simulation. Therefore, it has become necessary taking into account the distributed nature of the resistance, capacitance, and inductance, extraction of coupled RLC-networks with many lumps has [2].

2. SIMULATION METHODS

In this paper, we propose a method for the calculation of parasitics and the extraction of the distributed RLC circuit models from multi-level interconnects for circuit simulation. Figure 1 shows a schematic diagram illustrating the workflow of our extraction method. Referring to figure 1, our approach starts with partitioning the large layout into small sub-layouts.

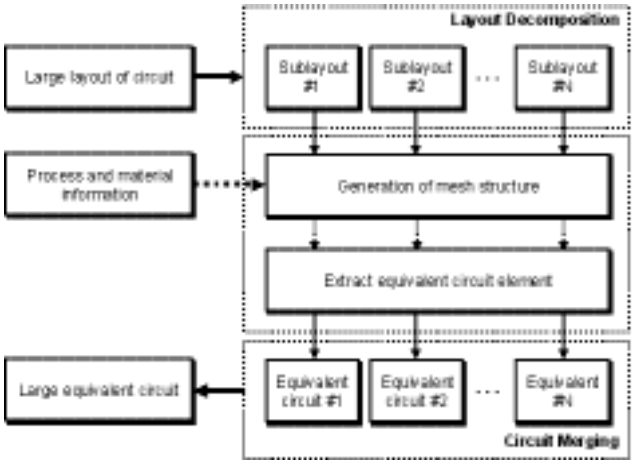


Figure 1: Schematic diagram illustrating the workflow.

2.1 Distributed RLC Circuit Model

After the whole circuit is divided into sub-layouts, the extraction of an RLC circuit model begins with fracturing of each sub-layout into a set of electrical node segments, resistive segments, and capacitive segments. Figure 2 shows an example illustrating our fracturing rules. An exemplary three-dimensional structure is shown in figure. 2 (a). Figure 2 (b) illustrates the method of the electrical node segmentation. Electrical node segments will be generated at edge regions (A, F, G, J, K, N, O, R), corner regions (C, D), and regions (B, D H, I, L, M, P, Q) that is either intersected or connected to via. The boundary condition is

imposed at each electrical node segment for a finite element method. The resistive segments and capacitive segments are shown in figure 2 (c) and 2 (d), respectively. The resistive segment is defined in the remaining structure after generating electrical node segments. The resistive segments are used to calculate resistance and inductance parameter of the RLC-network. The defined electrical node and resistive segments are used to define capacitive segments. Each capacitive segment is composed of each electrical node segment and halves of resistive segment connected to the electrical node segment. The capacitive segments are used to calculate capacitance parameter of RLC-network. In our approach, we assume that each capacitive segment has the same level of potential, and each resistive segment has a uniform current distribution for the calculation of parasitic capacitance, resistance, and inductance.

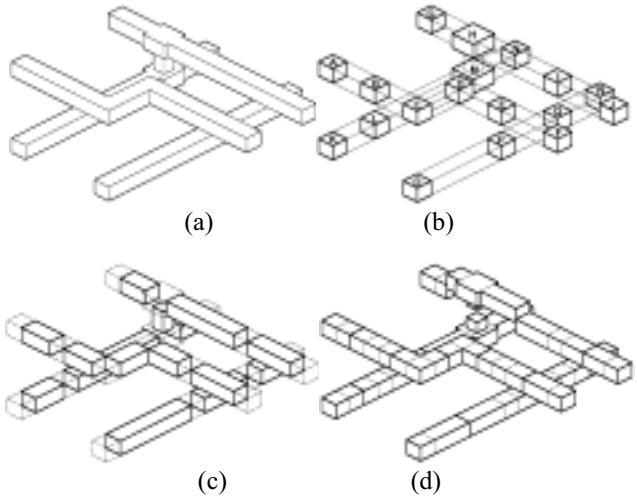


Figure. 2: (a) An exemplary structure illustrating our fracturing rules. (b) Electrical node segments are generated each regions of interconnects, thereafter, (c) resistive segments and (d) capacitive segments are defined.

In our model, each resistive segment has one resistance and one self-inductance. Mutual inductances are considered between resistive segments. Each capacitive segment has one self-capacitance and coupling capacitances between other capacitive segments.

2.2 Numerical Method

In order to extract resistances, inductances, and capacitances in the integrated circuits numerically, two independent quasi-static solutions of Maxwell's equation, equation (1) and equation (2), have to be solved numerically over dielectrics and conductors, respectively.

$$\nabla \cdot (\varepsilon(x,y,z) \nabla \phi_D(x,y,z)) = 0 \quad (1)$$

$$\nabla \cdot (\sigma(x,y,z) \nabla \phi_C(x,y,z)) = 0 \quad (2)$$

where, ε and σ are material constant, permitivity and electrical conductivity, respectively. Further, ϕ_D and ϕ_C are potential distribution in dielectrics and conductors as a function of position, respectively.

For the numerical calculation of the potential in dielectrics and conductors, the method of Ritz is applied. Therefore, the following variational formulations are used. Equation (1) and equation (2) can be formulated as equation (3) and equation (4), respectively.

$$I_D = \varepsilon_0 \int_{V_D} \varepsilon_r(x,y,z)[(\frac{\partial \phi_D}{\partial x})^2 + (\frac{\partial \phi_D}{\partial y})^2 + (\frac{\partial \phi_D}{\partial z})^2]dV \quad (3)$$

$$I_C = \int_{V_C} \sigma(x,y,z)[(\frac{\partial \phi_C}{\partial x})^2 + (\frac{\partial \phi_C}{\partial y})^2 + (\frac{\partial \phi_C}{\partial z})^2]dV \quad (4)$$

In equation (3) and equation (3), I_D, I_C denotes the total minimum energy of electric field stored in the dielectrics and the minimal power loss in the conductors.

Using the quasi-static strategy, we calculate potential distribution using Ritz method on dielectrics and conductors and thereby the current distribution is calculated from the calculated potential distribution over the conductors. Quasi-static strategy is applicable when the geometric dimensions of the simulated structure are small compared to the wavelength in the direction perpendicular to the signal propagation [3].

Capacitance and resistance can be extracted from electric energy and power loss at the given potential distribution, respectively. Inductance can be extracted from the numerical integration of Neumann formula. In order to integrate Neumann formula numerically, we use third order direct method of five points [4].

3. SIMULATION AND RESULTS

In order to extract RLC circuit model, we developed FEM solver to calculate the resistances, inductances, and capacitances for arbitrary three-dimensional interconnect structures. Also, a graphic input interface is developed to facilitate the specification and verification of the structure geometry [6, 7, 8]. The output parasitics are stored according to the convention of SPICE net-list and are ready for next-step circuit simulation and analysis.

In this paper, a sampler circuit was chosen to verify the validity of our approach. Figure 3 illustrates the exemplary layout of the sampler having 24 transistors, which is implemented with a 3.3 V CMOS technology with 0.3 μm, 1 poly and 3 metal interconnection lines. The width of metal 1 is 0.32 μm, while that of the other metal layers is 0.4 μm. The layout of the sampler has been decomposed into three small sub-layouts.

Figure 4 shows one of the sub-layouts and its simulation structure having tetrahedral mesh for extracting resistances, capacitances and inductances. In figure 4 (b), the

simulation structure includes 31 electrical node segments and capacitive segments and 21 resistive segments.

Figure 5 (a) and 5 (b) exhibits the calculated potential distribution on dielectrics and conductors, respectively. The number of nodes for FEM calculation was 68,115 with 375,624 tetrahedrons. The required CPU time for solving the potential distribution on dielectrics and conductors was approximately 10 minutes. For parasitics, resistance, capacitance and inductance, it took approximately 1 hour on ULTRA SPARC 10 workstation. In order to extract parasitics of the sub-layout, the metal is assumed to be aluminum and electric conductivity of poly, WSi_2, and metal is 0.001 $(\mu\Omega m)^{-1}$, 0.030 $(\mu\Omega m)^{-1}$, and 0.357 $(\mu\Omega m)^{-1}$, respectively. Dielectric constants of dielectrics are assumed to be 3.9 and 7.9, respectively. The magnetic permeability of conductor is assumed to be 0.9×10^{-5} (H/m).

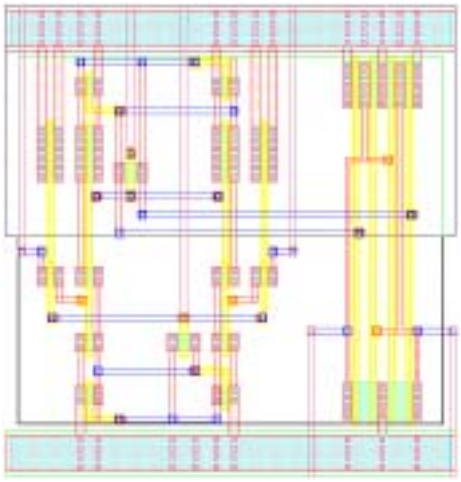
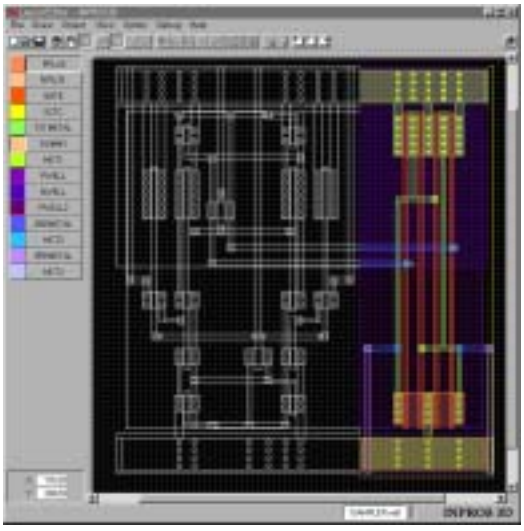
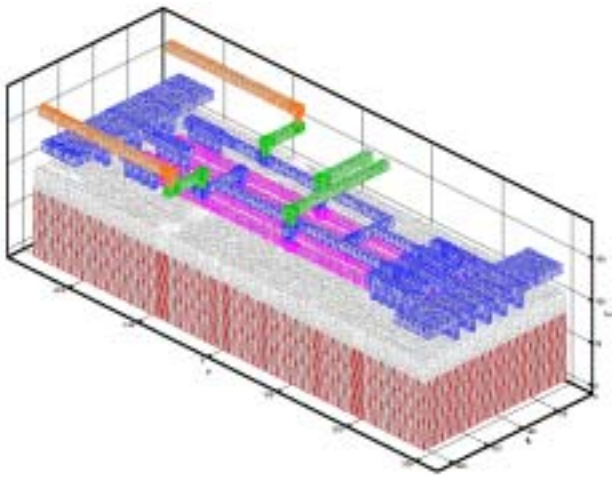


Figure. 3: Exemplary layout of the sampler having 24 transistors for a 3.3 V CMOS technology with 0.3 μm, 1 poly and 3 metal interconnection lines.

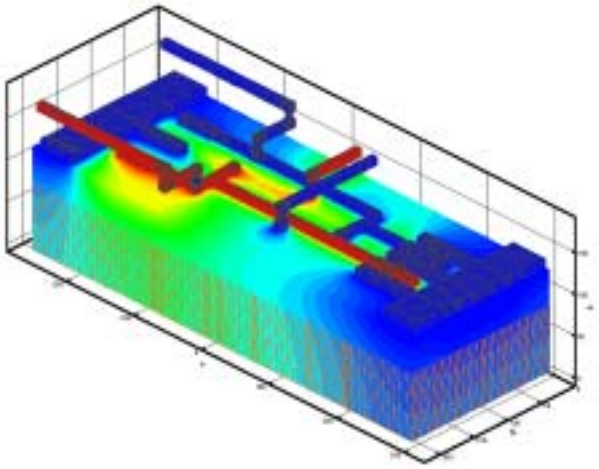


(a)

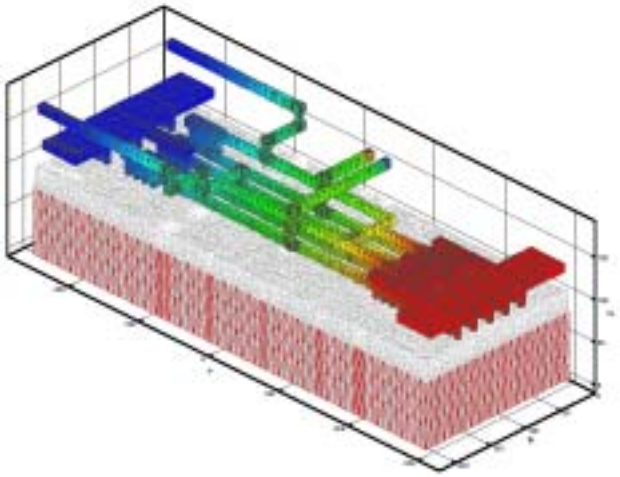


(b)

Figure 4: (a) One of sub-layouts and (b) simulation structures having tetrahedral mesh for extracting resistances, capacitances and inductances.



(a)



(b)

Figure 5: Calculated potential distribution on (a) dielectrics and (b) conductors

Figure 6 shows the net-list of the ideal sampler circuit and one of sub-circuits considered for the calculation of parasitics. Using HSPICE simulation on the net-list, the result in accordance with our approach was compared with Dracula RCX. Figure 7 shows the result of HSPICE simulation. The marked line is signal voltage at checkpoint shown in figure 6 (a). Referring to figure 7, our approach (B) provides a little bit larger time-constant and more voltage drop, because the calculated parasitics of our approach considers three-dimensional effect. Especially, since the simulation structure under consideration planar, the resistive segments are found to be after fracturing. Therefore, the magnitudes of the parasitic resistances are similar to those of the analytic method. Since the capacitive segments are of three-dimensional shape in spite of the fracturing into small segments, the three-dimensional behavior of capacitance is inherently taken into account. Although, the difference of the operational signal and the inductive effect were found to be small, was no miss operation existed. As the speed of integrated circuits increases into GHz region, it is very crucial to take the parasitics into account for the accurate simulation of the speed of chip operation. Furthermore, since the analytic approach generates a reasonably accurate model, can hybridize the analytic method with the numerical method for extracting parasitics with reduced simulation time.

4. CONCLUSIONS

In this paper, we proposed a method for extracting a distributed RLC circuit model from a complex three-dimensional interconnect structure. We have employed the layout-fracturing algorithm for generation of a distributed RLC circuit model. The proposed algorithm divides layout into three types of segments. These segments define the simulation domain and the boundary condition for extracting the parasitics in the distributed RLC network. A sampler circuit was chosen to verify the validity of our method. The layout of sampler circuit was fractured into 21 resistive segment, 31 electrical node segments and capacitive segments. For the finite element calculation of parasitics, a total of 68,115 nodes are generated with 375,624 tetrahedrons and it took approximately one hour on ULTRA SPARC 10 workstation. Our approach provides a little bit larger time-constant and more voltage drop, because the calculated capacitance of our approach considers three-dimensional shape. However, since the simulation structure under consideration is planar, the magnitudes of the parasitic resistances are similar to those of the analytic method. Therefore, our method can be hybridized with the analytic method for reducing simulation time.

ACKNOWLEDGMENT

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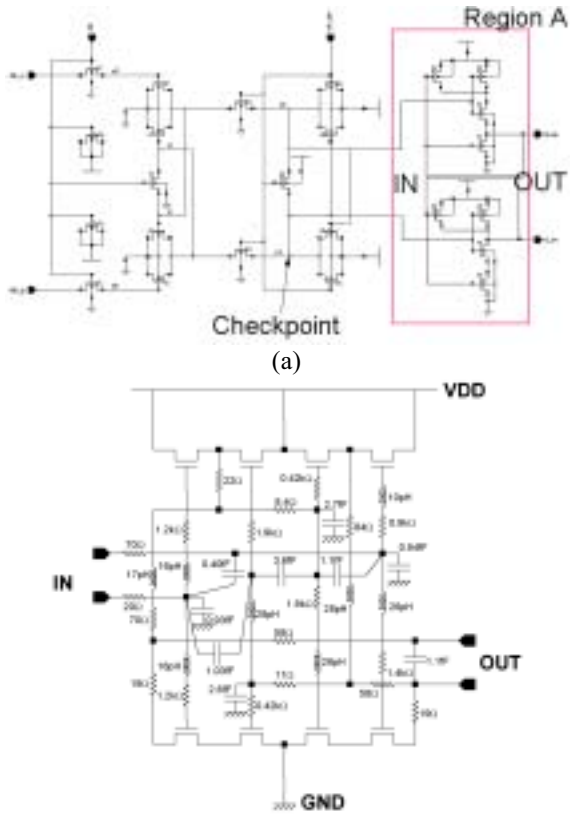

Figure 6: Net-list of (a) the ideal sampler circuit and (b) the sub-circuit of region A considered the calculated parasitics.

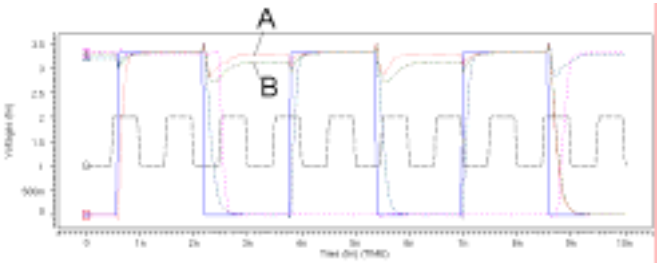

Figure 7: Result of HSPICE simulation of sampler circuit considered parasitics.

REFERENCES

[1] R. Wu et al., IEDM Trans. MTT vol. 40, 263, 1992.
[2] J. Jin, The Finite Element Method in Electro-magnetics, John wiley, 1993.

[3] R. Sabelka et al., SISPAD 2000, 6, 2000.
[4] K. Bathe, Finite Element Procedures, Prentice hall, 1996.