Novel Computing Architecture on Arrays of Josephson Persistent Current Bits

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ABSTRACT

A superconducting qubit (or quantum bit), which consists of a micrometer-sized loop with three Josephson junctions, has two persistent currents of opposite direction as its two states. The states of the qubit can be brought into quantum coherence to perform quantum computing. Classical bits can also be obtained from these superconducting loops, making it possible to base a classical computer architecture. We study a novel computing structure based on these Josephson Persistent Current (PC) Bits, starting from elementary logic gates to a Random Access Memory (RAM). The investigation shows that the Josephson PC Bit technology would not surpass semiconductor technology in term of the device density, while it is a promising candidate for unltra-fast memory, which can be integrated with other technologies. The classical computer might also serve as pre and post processor for the quantum computing performed in the heart of the array. The Josephson PC circuits, therefore, seems a good vehicle for the study of the quantum computer paradigm.

Keywords: computing architecture, Josephson, circuit simulation, classical computing, quantum computing

1 INTRODUCTION

Silicon-based CMOS circuitry has dominated microelectronics for decades. Besides the continuous miniaturization of the elements used to construct computers, ultra-dense and fast systems based on other technologies are also envisioned and proposed. The quantum computer is probably the ultimate objective of this endeavor. Various physical systems were proposed for quantum computing. Among those mesoscopic superconducting circuits of ultra-small Josephson junctions, which can be produced by modern lithography, appear promising for integration in electronic circuits and large-scale applications. Recently, the quantum superposition of two macroscopic persistent-current states on superconducting Josephson circuits was detected and measured [1]. Thus, the proposed qubit (or quantum bit), which consists of a micrometer-sized loop with three Josephson junctions, is possible to be brought into quantum coherence to perform quantum computing.

Classical bits can also be obtained from these superconducting loops by increasing its critical current, making it possible to base a classical computing architecture on these Josephson Persistent-Current (PC) bits. In this paper we study a novel computing structure based on the Josephson (PC) Bits, starting from elementary logic gates to a Random Access Memory (RAM) design. The proposed classical parallel computer could also be a significant part in the realization of quantum computers, for the same device can be used for both classical and quantum computing [3]. Although the classical computing part could as well be done with conventional CMOS technology, the study on the Josephson PC circuits might bring us an insight that cannot easily be achieved with other spin based devices for quantum computers, because of the problems involved in combining them with conventional technology.

In the second section we present a close look at the Josephson PC circuit and focus on the properties we are interested in. In the following sections we discuss the design of a classical computing structure, from elementary logic gates to a Random Access Memory (RAM). Finally, some conclusions are drawn.

2 THE JOSEPHSON PC QUBIT/BIT

A Josephson PC qubit in principle consists of a loop with three Josephson junctions in series that encloses a magnetic flux Φ driven by an external magnet (Fig.1). In particular when the enclosed magnetic flux is close to half a superconducting flux quantum Φ_0 (=$h/2e$, where h is Planck's constant), the loop may have multiple stable persistent current states, and this system behaves as a particle in a double-well potential, where the classical states in each well correspond to persistent currents of opposite sign. The two classical states are coupled via quantum tunneling through the barrier between the wells, and the loop is a macroscopic quantum two level system. This system has two stable states $|0\rangle$ and $|1\rangle$ with opposite circulating persistent currents [1][2].

The qubit is operated by resonant microwave modulation of the enclosed magnetic flux by a superconducting control line. The superconducting control line is on top of the qubit, separated by a thin insulator. Measurement can be made with superconducting magnetometers [superconducting quantum interference devices (SQUIDs)] [2].

When the quantum tunneling does not take place, the system behaves classically so that on the loop there is a

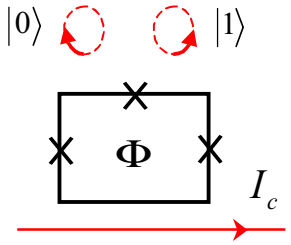

Fig. 1 A Josephson PC qubit

single stable current circulating clockwise or anti-clockwise. These two states serve as the bit for Boolean logic: 0 and 1. The states of this Josephson PC bit can be switched (activated or suppressed) by external magnetic flux. When the external flux is about half flux quantum ($1/2\,\Phi_0$), the bit is activated (0 or 1); when the external flux is removed, it is suppressed (neither 0 nor 1). The state of a bit (0 or 1), furthermore, depends on the sum of the external magnetic flux generated by the circulating currents on the surrounded loops: one slips to 0 (or 1) as the magnetic field shifts lower (or higher) than half flux quantum ($1/2\,\Phi_0$). The Josephson PC bits, therefore, can be coupled to perform logic functions, and more complicated circuits and systems could be built on them.

3 ELEMENTARY CLASSICAL LOGIC

The circuit with Josephson junctions can be produced by modern lithography. The advantage of solid state lithographed circuits is their flexibility in the parameters and the layout of the circuit. In the classical regime, two or more PC bits can be coupled to each other by the interaction of the magnetic field generated by the circulating currents. The state of a bit (0 or 1) depends on the magnetic flux generated by the circulating currents, i.e. the states, of all the bits it is coupled to. As soon as a PC bit is activated, the magnetic flux from all the surrounded magnetic sources are added and one slips to the "addition" of the states of all those it is coupled to. An inverter (NOT) (Fig.2) is obtained by coupling two of the bits and a Not Majority Vote (NMV) gate (Fig.3) by coupling more.

Quantum-effect devices will probably have more variability in their characteristics than the earlier microstructure counterparts. Therefore the topology of the Josephson PC bit circuits has to be delicately designed. We started simulation with fundamental elements, namely the inverter and NMV gate, to make them robust in practical implementation. The work was basically done with a package, FastHenry, which computes the frequency dependent self and mutual inductances and resistances between conductors of complex shape. Given the inductance values, the coefficients of effective Hamiltonian, which exhibit the interaction between the persistent-current loops, were approximately calculated, with the linear approximation to the persistent currents applied [4].

Two different schemes for a two-bit inverter were simulated respectively under certain physical parameters. An inverter was firstly proposed by coupling two superconductive loops directly through magnetic interference. In the second scheme, the two loops were coupled through a superconductive flux transporter, which was placed on top of them and insulated by a thin layer (Fig.2). The inductive influence from control current lines, which is on top of the transporter, is also considered. In order to manipulate a PC bit independently, the control line should be strongly coupled with one while weakly coupled with the other. The inductances obtained from the latter simulation are shown in Table 1. The mutual inductance between a PC bit loop and the control line is 2.3pH, which is about two orders larger than that between the control line and the other loop, 0.026~0.028pH. The mutual inductance between the transporter and the PC loops is 9.7pH, while the mutual inductance between the two loops is about 0.069pH. With the parameters suggested in [2] and the inductance matrix obtained from our simulation, the coefficient of the effective Hamiltonian H, which stands for the interaction between the two PC loops, was calculated to be about 0.08 (in units of Josephson energy E_J), which was 5~6 times larger than that without the transporter. Thus

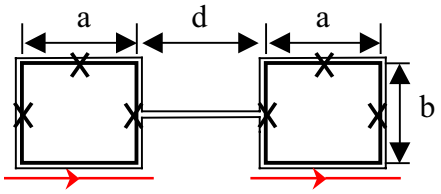

Fig.2 simulated inverter

Table 1. Mutual (self) inductance (pH) in the inverter circuit

	Transporter	Loop 1	Loop 2	Control line 1	Control line 2
Transporter	30	9.7	9.7	3.1	3.1
Loop 1	9.7	11	-0.069	2.3	0.028
Loop 2	9.7	-0.070	11	0.028	2.3
Control line 1	3.1	2.3	0.026	4.3	0.28
Control line 2	3.1	0.026	2.3	0.28	4.3

the simulation showed that the interaction between the PC loops was stronger and they are better coupled to each other with the facilitation of transporter.

In more complicated circuits, for example, the NMV gate, more factors are involved. To put the proposed NMV work properly, the wanted and unwanted coupling between all the components must be deliberatively arranged. The scheme shown in Fig. 3 was simulated with FastHenry, and it is expected to work reliably (probably some parameter tuning is needed). To completely and accurately describe the circuit, however, would be rather difficult, because of the large amount of parameters involved. In such a topology the NMV node serves as fan out circuit as well as NAND, NOR and NOT (inverter) by setting instruction bits. It works actually as a data processing unit, which could be the fundamental element for a large data processing network.

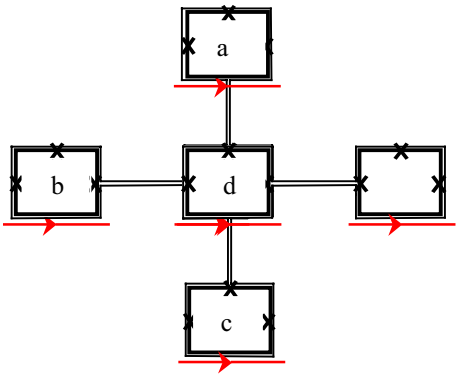

Fig.3 simulated NMV gate

Since the PC bits we discussed are all coupled to its nearest neighbors, the long-range communication seems a hard task. With the facilitation of a transporter, however, it could be possible to realize fast data propagating. Let's assume that a big transporter is put on top of a chain, which consists of a number of PC bits (Fig.4). This circuit was simulated with FastHenry, and we got the same value for the mutual inductance between the transporter and every PC loop. Since every PC bit in the chain interacted equally with other parts of circuit, all the cells are simultaneously switched, given a synchronous clock. A bit is quickly propagated to all the cells in a chain, as soon as it is injected into one of them in the chain. We estimate that the fast data propagating could be implemented on the PC bit arrays, provided that they are ideally fabricated.

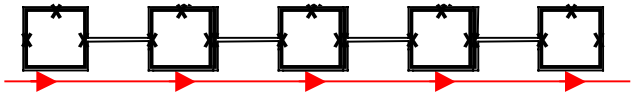

Fig.4 Fast data propagation

The fast data propagating makes it efficient to perform logic functions on the Josephson PC bit network. During each operation, instruction and data inputs are quickly propagated into the data bus of the network. Instructions are fed into the network as well in serial. The Josephson PC network is then configured into a custom computer to perform useful arithmetic and logic operations.

4 MEMORY DESIGN

It is arguable that the most important component of modern computing systems is not the processor, but the memory. Fortunately, the Josephson circuits own natural properties to be good memory cells, where information is stored as a persistent current. Fig. 5 shows an implementation of memory cell array on Josephson PC network with column (ca) and row (ra) addressing. A row addressing decoder is shown as well. To write a bit into a memory cell, we feed the bit into the array via data bus and select the cell with positive row and column addressing lines. The addressing lines are designed in such a way, that a cell is activated only when both of its row and column WRITE addressing (Wa) lines are positive. A memory cell can not be refreshed by either a row or a column addressing line independently. As soon as a cell is activated, a bit from the data bus is stored in. The cells that are not selected are not affected, because neither or only one of their addressing lines is positive. To read out the states, we activate the cell that is attached to the being-accessed memory cell, by selecting both the row and column READ addressing (Ra). Since the addressing lines are designed in such a way that the states of other cells in the same column are suppressed during reading, the selected one gets the bit from its adjacent memory cell, without interacting with its neighbors in the same column. The bit is then quickly shifted out via data bus.

A two-bit decoder is shown in Fig.5. Address signal arrives at a PC/DC converter, where the Persistent-Current (PC) signal is translated into DC signal and then transmitted into control current lines. These control lines are inductively coupled to the PC cells of the address decoders. A decoder consists of rows of PC cells. In each row the cell in one end is initially set to 1 or 0, and all the cells are coupled to its nearest neighbors. The control lines are designed in such a way, that a cell is activated or suppressed by positioning its control line on two sides of the cell. The set bit is then passed through the activated cell while blocked by the suppressed one. For any address signal, there is only one row in the decoder, capable of passing the PC signal from one end to the other. The decoded information is then transmitted into a PC/DC converter, where it is translated for the addressing in memory array.

The proposed memory architecture has the density of 25 MBits/cm^2, which cannot compete with the current Semiconductor technology (see Table 2), according to the International Technology Roadmap for Semiconductors [5]. As the operating could be extremely fast (clock rate up to

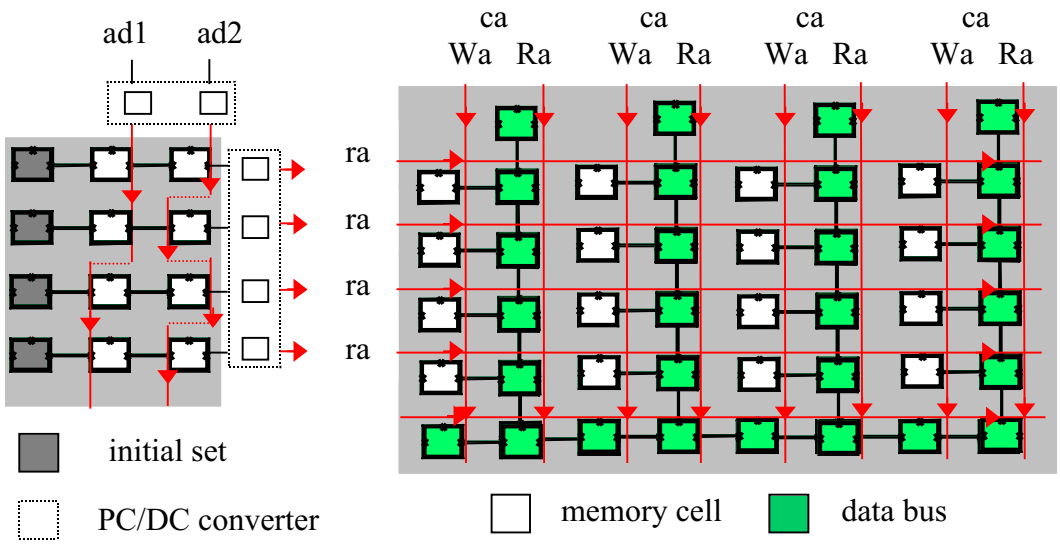

Fig.5 Josephson PC memory array with address decoder

100 GHz), and the power consumption would be extremely low, the Josephson PC memory appears a promising candidate for ultra-fast memory structure, and could be integrated with other technologies.

5 CONCLUSIONS

If the interconnections among the Josophson PC bits are well established, data processing, transmitting and storing can be effectively done with the switching of the control currents. It is possible, therefore, to build a powerful computer out of the Josephson PC loops. Because of the electromagnetic interaction among the large amount of devices, however, the complexity on manipulating the control currents makes it rather hard to build complicated logic circuits, although the operating could be extremely fast, and the power consumption would be extremely low. Instead the Josephson PC memory, although bulky, appears a promising candidate for ultra-fast memory structure, and they could be integrated with other technologies to serve as components for a hybrid supercomputer.

Table.2 Josephson PC and semiconductor technology

	Gate length (um)	Memory (MBits/cm^2)	On-chip clock (GHz)
Semiconductors in 2002	0.08	700	2.5
Josephson PC technology	4	25	100

The classical Josephson PC bit network might also serve as the pre and post-processor of the quantum network in the heart of the array [3]. Because classical and quantum computing based on the same device can be studied now simultaneously, which is impossible in certain circumstances, e.g. the ensemble spin-based quantum computer, the architecture of arrays of Josephson PC qubit/bit seems a good vehicle for studying the quantum computer paradigm, independently from the question whether the Josephson PC loops will be the ultimate implementation device.

6 ACKNOWLEDGEMENT

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