

# Development of MEMS Vertical Planar Coil Inductors Through Plastic Deformation Magnetic Assembly (PDMA)

Jinghong Chen\*, Jun Zou\*\*, Chang Liu\*\* and Sung-Mo (Steve) Kang\*\*\*

\* Agere Systems, Holmdel, NJ 07733

\*\* Department of Electrical and Computer Engineering,

University of Illinois at Urbana-Champaign, Urbana, IL 61801

\*\*\* Jack Baskin School of Engineering, University of California, Santa Cruz, CA 95064

## ABSTRACT

This paper presents the results of the development of a vertical planar coil inductor. The planar coil inductor is first fabricated on silicon substrate and then assembled to the vertical position by using a novel 3-Dimensional bath-scale self-assembly process (Plastic Deformation Magnetic Assembly (PDMA)). Inductors of different dimensions are fabricated and tested. The S-parameters of the inductors before and after PDMA are measured and compared, demonstrating superior performance due to reduced substrate effects and also increased substrate space savings for the vertical planar coil inductors.

**Keywords:** MEMS, planar coil inductor, quality factor, PDMA, resonance frequency.

## 1 INTRODUCTION

With the development of integrated wireless communication systems, on-chip inductors with satisfactory performance (enough quality factor and self-resonant frequency) are required. However, the conventional planar coil inductor suffers from substrate losses and parasitics since it is directly fabricated onto conductive substrate over a very thin dielectric layer [1].

In recent years, much effort has been made to improve the performance of planar coil inductors. Metal materials with higher conductivity or thicker metal layers are utilized to decrease the resistance of the coil. Meanwhile, different methods are proposed to reduce the substrate loss and parasitics, including removing the substrate underneath the inductor [2], applying a thick polyimide layer to separate the inductor farther away from the substrate [3], etc.

More recently, planar coil inductors levitated above the substrate are realized using a sacrificial metallic mode (SMM) process [4]. 3-Dimensional solenoid on-chip inductors developed by using 3-D laser lithography or surface micromachining technology have also been demonstrated [5,6].

This paper reports vertical planar coil inductors developed by using a novel 3-D self-assembly process-Plastic Deformation Magnetic Assembly (PDMA). Experimental results show that the vertical planar coil inductor suffers less substrate loss and parasitics than the conventional horizontal counterparts, and thus can achieve a higher quality (Q) factor and self-resonant frequency. Another major advantage of the vertical inductors is that they have almost zero footprints and thus occupy much smaller substrate space.

## 2 PLASTIC DEFORMATION MAGNETIC ASSEMBLY (PDMA)

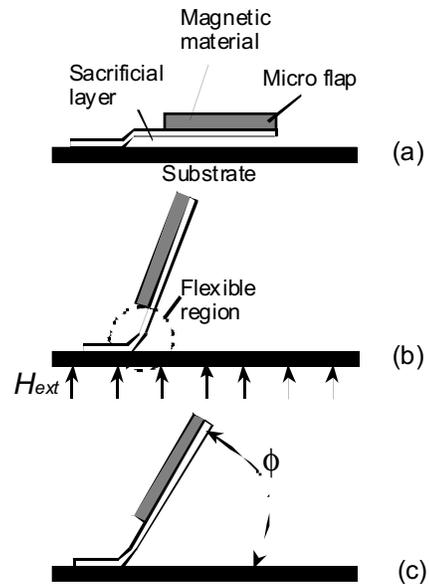


Fig. 1 A schematic illustration of a Plastic Deformation Magnetic Assembly process (PDMA)

PDMA is the key technology to realize the vertical planar coil inductors. A detailed discussion of this assembly process will be presented in other publications. A brief introduction of PDMA is given below by using a cantilever beam as an example. Note that the region near the fixed end is intentionally made more flexible. First, a

cantilever beam with a piece of magnetic material attached to its top surface is released from the substrate by etching away the sacrificial layer underneath (Fig. 1(a)). Next, a magnetic field  $H_{ext}$  is applied, the magnetic material piece is magnetized and the cantilever beam will be rotated off the substrate by the magnetic torque generated in the magnetic material piece (Fig. 1(b)). If the structure is designed properly, this bending will create a plastic deformation in the flexible region. The cantilever beam will then be able to remain at a certain rest angle ( $\phi$ ) above the substrate even after  $H_{ext}$  is removed (Figure 1(c)). By using ductile metal (e.g. gold) in the flexible region, a good electrical connection between the assembled structure and the substrate can be easily achieved, which is suitable for RF applications.

After the vertical assembly, the structures can be further strengthened and the magnetic material can be removed if necessary. If the magnetic field is applied globally, then all the structures on one substrate can be assembled in parallel.

### 3 DESIGN AND FABRICATION

The core structure of the vertical planar coil inductor is identical to the conventional horizontal one, which consists of two metal layers and one dielectric layer between. As a general rule, high conductivity metal and low loss dielectric material should be used. In addition to this requirement, the structure of the inductor should facilitate the implementation of PDMA.

The vertical planar coil inductor utilizes one-port coplanar waveguide (CPW) configuration with 3 test pads (Ground-Signal-Ground) with a pitch of  $150\mu\text{m}$ . The three test pads also serve as the anchor of the vertical inductors on the substrate.

#### 3.1 Material Consideration

Gold is used as the material for the bottom conductor (the coil). Gold is a ductile material with high conductivity. It is an ideal plastic deformation material for the implementation of PDMA. Copper is selected as the material of the top conductor (the bridge). Copper is also a high conductivity metal and its processing is compatible with the gold bottom conductor during the fabrication.

Silicon oxide and nitride are good dielectric materials available in silicon IC process. However, they are not suitable for vertical planar coil inductors due to high internal stress and poor adhesion on metal surface.

CYTOP<sup>®</sup> amorphous fluoro-carbon polymer is selected as the dielectric spacer of the vertical inductors. The electrical properties of CYTOP<sup>®</sup> film are similar to those of

Polyimide and Teflon<sup>®</sup>. However, it has a better adhesion on metal surfaces and chemical stability.

In order to implement PDMA, Permalloy (NiFe) is electroplated onto the surface of the gold and copper structures. The Permalloy layer will provide the magnetic force necessary for PDMA and enough stiffness to the inductor structure in the vertical position.

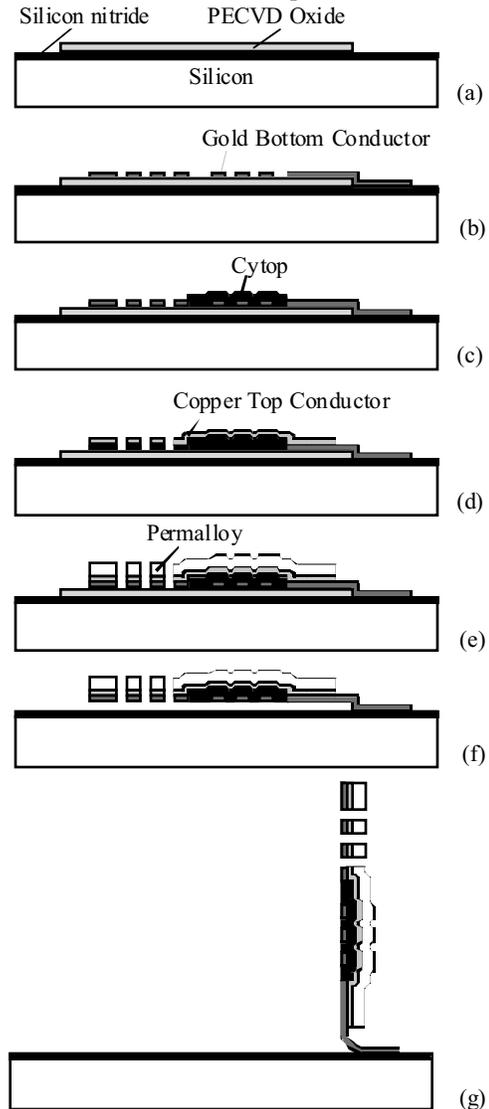


Fig. 2 A schematic illustration of the fabrication and PDMA assembly of vertical planar coil inductors.

#### 3.2 Fabrication Process

A brief illustration of the entire fabrication and assembly process is shown in Fig. 2. The substrate is a silicon wafer with a  $0.6\mu\text{m}$ -thick nitride layer on top. The fabrication is conducted in the following steps:

- (a) A  $0.5\mu\text{m}$ -thick silicon oxide layer is deposited and patterned to serve as the sacrificial layer for PDMA.

- (b) A  $0.5\mu\text{m}$ -thick gold layer is deposited onto the substrate (with sacrificial layer underneath) and patterned to make the bottom conductor (coil) of the inductor.
- (c) A  $2.5\mu\text{m}$ -thick CYTOP<sup>®</sup> film is spun onto the gold layer and patterned to make the dielectric spacer.
- (d) A  $1.5\mu\text{m}$ -thick copper layer is deposited and patterned to make the upper conductor (bridge) of the inductor.
- (e) A  $5\mu\text{m}$ -thick Permalloy layer is electroplated onto the copper and gold surface.
- (f) The oxide sacrificial layer is etched and the inductor structure is released from the substrate.
- (g) The entire inductor structure is assembled into vertical position using PDMA.

Scanning electron micrographs of a  $4.5\text{nH}$  planar coil inductor before and after PDMA are shown in Fig. 3.

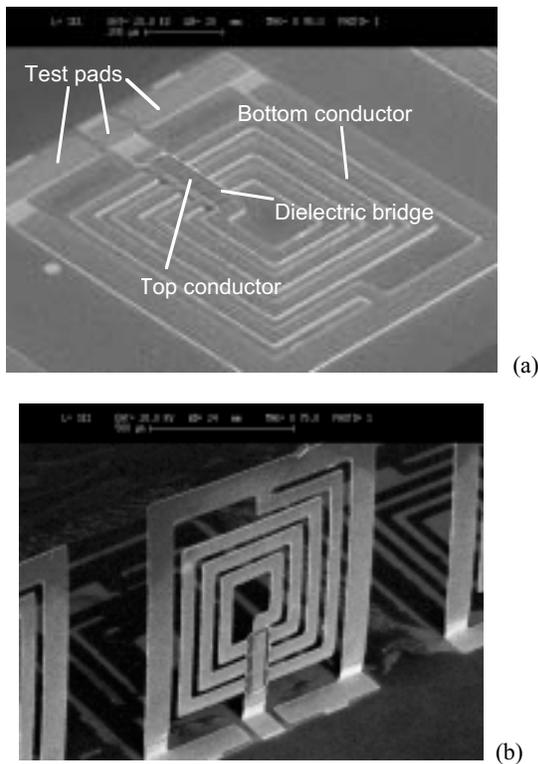


Fig. 3 (a) A scanning electron micrograph of a planar coil inductor fabricated on the substrate surface before the PDMA assembly; (b) A scanning electron micrograph of the same inductor after the PDMA assembly.

#### 4 TESTING AND MEASUREMENT RESULTS

The  $S_{11}$  parameter of the fabricated vertical planar coil inductors is measured from 50 MHz to 4GHz using an HP<sup>®</sup> 8510C network analyzer. The  $S_{11}$  parameter is first measured while the inductors are on the silicon substrate

before PDMA. Next, the inductors are assembled to the vertical position using PDMA and the  $S_{11}$  measurement is repeated. The  $S_{11}$  parameter of inductors with identical designs fabricated on Pyrex<sup>®</sup> glass substrate is also measured for comparison.

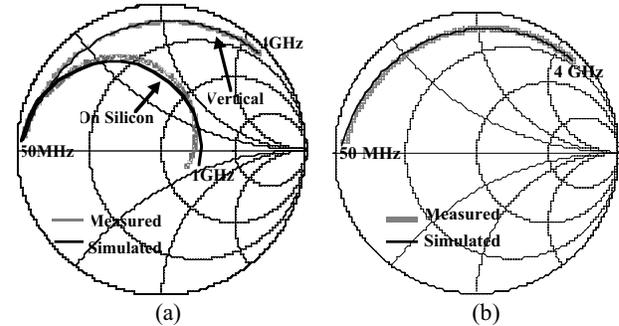
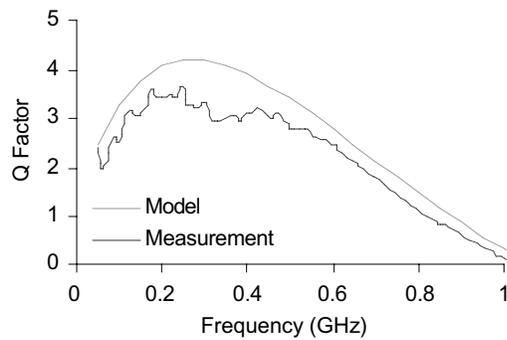


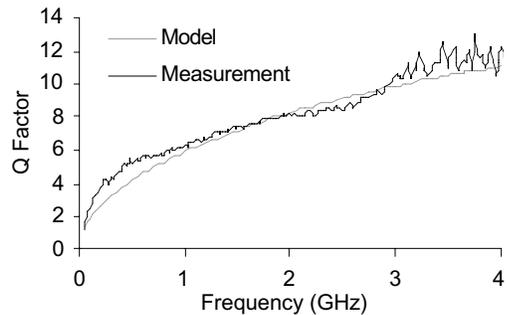
Fig. 4 (a) A Smith chart showing the simulated and measured  $S_{11}$  parameter results of the planar coil inductor shown in Fig. 3 before and after PDMA. (b) A Smith chart showing the simulated and measured  $S_{11}$  parameter results of an inductor with identical design fabricated on glass substrate. The inductance of both inductors is  $4.5\text{nH}$ .

Fig. 4 (a) shows the simulated and measured  $S_{11}$  parameter results of the planar coil inductor shown in Fig. 3. The test pads feeding the inductors on which probing occurs are de-embedded. Fig. 4(b) shows the simulated and measured  $S_{11}$  parameter results of an inductor with identical design inductor fabricated on Pyrex<sup>®</sup> glass substrate. The test pads are not de-embedded since the inductor is on glass substrate and the de-embedment has little effect. The simulated data is obtained by using a compact circuit model for planar coil inductor presented in [1]. The quality factor (Q) as a function of frequency extracted from both the simulated and the measured  $S_{11}$  parameter results is plotted in Fig. 5. When the planar coil inductor is on the silicon substrate, it has a peak Q factor of 3.5 and self-resonant frequency of 1GHz. When the inductor is in the vertical position after the PDMA assembly, the peak Q factor increases to 12 and the self-resonant frequency goes well above 4GHz, which are close to those of the inductor on glass substrate.

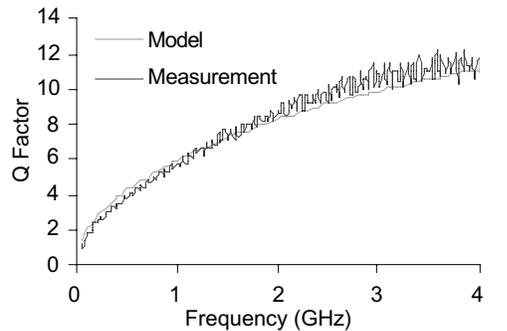
For the planar coil inductors fabricated on silicon (before assembly), a large insulator capacitance and the substrate resistance dominate at higher frequencies, which leads to a self resonate frequency of about 1GHz. Once the inductors are assembled into the vertical position, the substrate loss and capacitance are effectively removed, which leads to the improvement in the inductor performance. Furthermore, for frequencies far below 1 GHz (where substrate effects are negligible), the glass and silicon inductor measurements correspond exactly, as expected.



(a)



(b)



(c)

Fig. 4 The quality factor of the planar coil inductor extracted from the simulated and measured  $S_{11}$  parameters: (a) the inductor on silicon before PDMA; (b) the inductor in vertical position after PDMA; (c) an inductor with identical design on glass substrate.

## 5 DISCUSSIONS

- 1) In this work, oxide is used as the sacrificial material for PDMA. Sometimes, oxide is used as the dielectric for IC devices on the same substrate and thus cannot be removed. In this case, the oxide sacrificial layer can be substituted by other materials, e.g. photo resist.
- 2) In order to facilitate the measurement, the vertical planar coil inductors tested are not strengthened after PDMA. However, the inductor structure can be strengthened after PDMA by using different methods (e.g. Parylene

coating) to achieve the necessary stiffness and robustness.

- 3) While the Q factor of vertical planar coil inductors can be improved by depositing thicker metal layers during the fabrication, experiments are also being conducted to explore various methods to thicken and strengthen the metal layers of the planar coil inductors while they are in the vertical position after the PDMA assembly.

## 6 CONCLUSIONS

Vertical planar coil inductors have been achieved by using a novel 3-D assembly-Plastic Deformation Magnetic Assembly (PDMA). Vertical planar coil inductors offer two major advantages over conventional on-substrate ones: they occupy much smaller substrate space and suffer less substrate loss and parasitics.

The proposed fabrication and assembly process of the vertical planar coil inductor is compatible with the standard IC fabrication process, and is therefore suitable for various RF ICs.

## REFERENCES

- [1] C. P. Yue and S. S. Wong, "Physical modeling of spiral inductors on silicon," *IEEE Trans. On Electron Devices*, vol. 47, no. 3, March, 2000, pp. 560-568.
- [2] M. Ozgur, M. Zaghoul, and M. Gaitan, "High Q backside Micromachined CMOS inductors," *ISCAS'99. Proceedings of the 1999 IEEE International Symposium on Circuits and Systems*, vol.2, 1999, pp.577-80.
- [3] B. K. Kim, B. K. Ko, and K. Lee, "Monolithic planar RF inductor and waveguide structures on silicon with performance comparable to those in GaAs MMIC," *IEDM Tech. Dig.*, 1995, pp. 717-720.
- [4] J. B. Yoon, C. H. Han, E. Yoon and C. K. Kim, "High-performance three-dimensional on-chip inductors fabricated by novel micromachining technology for RF MMIC," *IEEE MTT-S Digest*, 1999, pp 1523-26.
- [5] D. Young, V. Malba, J. Ou, A. Bernhardt, and B. Boser, "Monolithic high-performance three-dimensional coil inductors for wireless communication applications", *IEDM Tech. Dig.*, 1997, pp. 67-70.
- [6] J. B. Yoon, B. K. Kim, C. H. Han, E. Yoon, K. Lee and C. K. Kim, "High-performance electroplated solenoid-type integrated inductor (SI2) for RF applications using simple 3D Surface micromachining technology," *IEDM Tech. Dig.*, 1998, pp.544-547.