New Compact Model for Generation Drain Current Transients in Weak and Moderate Inversions of Submicron Floating-Body PD SOI MOSFETs

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ABSTRACT

In this paper, generation-type drain current transients, in advanced (down to 50nm gate-length) floating-body PD SOI MOSFETs are investigated by 2D numerical simulation in weak inversion operation. An original compact analytical model is derived for the pure transient weak inversion operation and validated on both elementary and realistic 2D structures. The proposed sub-threshold transient compact model allows accurately to predict the influence of the generation lifetime, surface velocity (or interface state density), oxide thickness and substrate doping on floating-body related transient behavior and duration, which is essential for advanced transistor optimization and subsequent circuit applications. Moreover, our model is a unique, robust tool for the electrical characterization of submicron SOI transistors since it allows the carrier lifetime extraction independently on the channel carrier mobility and device effective gate length.

Keywords: carrier lifetime, Silicon-On-Insulator, weak inversion, submicron MOSFET, compact modeling.

1 INTRODUCTION

Nowadays very large scale integration (VLSI) design being focused on the high speed, low power, low-voltage, and mixed-signal applications, the accurate modeling of the submicron MOSFETs becomes a very important issue. Moreover, as the supply voltage for mixed-signal circuits is reduced towards 1.2 V, the bias of transistors at low current levels, below the onset of the strong-inversion from the weak-inversion region, becomes very popular. Particularly, SOI transistors appear to be extremely adapted for such a low-current/low-voltage bias regimes for which there is a real lack of accurate compact models [1].

This paper deals with the very critical compact modeling of the transient regimes of floating-body partially depleted (PD) SOI MOSFETs (weak and moderate inversions) induced by the step-functions applied on one of the transistor gates since the opposite is kept at constant bias. The induced ‘generation’ transient is analytically modeled in two different switching regimes that correspond to: (I) real transistor operation switching (*on* to *off* state) and (II) to a characterization-dedicated method (similar to the deep depletion pulsing).

2 WEAK INVERSION GENERATION-TRANSIENT COMPACT MODEL

The weak inversion generation-transient regime in a double-gate floating body PD SOI MOSFET is observed when biasing one gate in the sub-threshold region and by applying a step-function which drives the opposite gate into accumulation [1-2]. The induced charge non-equilibrium results in a drain current transient, which essentially reflects e^--h^+ pair generation in the extension of the generation region. Note that a similar generation transient is obtained when switching the front gate from strong or moderate inversion into weak inversion (part of a typical *switching off* regime). The equations that describe the time evolution of majority and minority carriers, in a n-channel PD SOI MOSFET, are:

$$\frac{1}{qn_i}\left(\frac{dQ_d(t)}{dt}+\frac{dQ_{acc}(t)}{dt}\right)=\frac{W(t)-W_\infty}{\tau_{geff}}+S_{eff} \qquad (1)$$

$$-Q_d(t)-Q_{inv}(t)=C_{ox1}\,(V_{G1}-V_{FB1}-\psi_{S1}(t)) \qquad (2)$$

$$Q_d(t)=-qN_AW(t)=-\sqrt{2q\varepsilon_sN_A(\psi_{S1}(t)-V_B(t))} \qquad (3)$$

$$Q_{acc}(t)=-C_{ox2}\,(V_{G2}-V_{FB2}-V_B(t)) \qquad (4)$$

where Q_d, Q_{acc} and Q_{inv} are the depletion, accumulation and inversion charges, W is the depletion region depth, τ_{geff} and S_{eff} are the generation lifetime and surface generation velocity, respectively and V_B is the neutral floating body potential. Subscripts 1 and 2 apply for the front and back interfaces, respectively. The main features of a weak inversion transient, in contrast with a strong inversion, are: $Q_{inv} \ll Q_d$ and a time-varying surface potential, $\psi_S(t)$. Eliminating V_B between eq. (1)-(4) gives:

$$-\frac{N_A}{n_i}\left[1+\frac{C_{ox2}}{C_{ox1}}+\frac{C_{ox2}}{\varepsilon_s}W(t)\right]\frac{dW}{dt}=\frac{W(t)-W_\infty}{\tau_{geff}}+S_{eff} \qquad (5)$$

With conventional expressions of the drain current and inversion charge in weak inversion regime, eq. (5) becomes:

$$\frac{C_{ox1}}{qn_i\beta}\left[1+\frac{C_{ox2}}{C_{ox1}}-\frac{C_{ox1}C_{ox2}}{q\varepsilon_s\beta N_A}\ln\frac{I_D}{I_k}\right]\frac{1}{I_D}\frac{dI_D}{dt}= \tag{6}$$

$$=\frac{C_{ox1}}{q\beta N_A\tau_{geff}}\ln\frac{I_\infty}{I_D}+S_{eff}$$

where

$$I_k=\frac{\mu Z}{\beta^2 L}\sqrt{\frac{q\varepsilon_s N_A}{3\phi_F}}\,(1-e^{-\beta V_D})\,e^{\beta(V_{G1}-V_{FB1}-2\phi_F)}$$

and β=q/kT. For conventional parameters of SOI devices eq. (6) could be further simplified:

$$\underbrace{\frac{C_{ox1}}{qn_i\beta}\frac{1}{I_D}\frac{dI_D}{dt}}_{LHS}=\underbrace{\frac{C_{ox1}}{q\beta\,N_A}\ln\frac{I_\infty}{I_D}}_{RHS}\frac{1}{\tau_{geff}}+S_{eff} \tag{7}$$

Plotting the left side LHS(t) of eq. (7) as a function of RHS(t) gives τ_{geff} (slope) and S_{eff} (intercept with vertical axis). Moreover, integrating eq. (7) from t=0 to $t=t_\infty$ gives the unique analytical expression of the drain current transient in the weak inversion operation:

$$I_D(t)=I_\infty\exp\left\{\frac{q\beta N_A\tau_{geff}S_{eff}}{C_{ox1}}\left[1-\exp\left(\frac{n_i}{N_A\tau_{geff}}(t_\infty-t)\right)\right]\right\} \tag{8}$$

where t_∞ can be calculated as:

$$t_\infty=\frac{N_A\tau_{geff}}{n_i}\ln\left[1-\frac{C_{ox1}}{q\beta N_A\tau_{geff}S_{eff}}\ln\frac{I_0}{I_\infty}\right] \tag{9}$$

and I_0 is the drain current value at the beginning of the transient, analytically calculated with $\psi_S=\psi_F/2$. At the best of our knowledge, this is the first full compact transient model reported in weak inversion.

3 MODEL EXTENSION IN MODERATE AND STRONG INVERSIONS

In order to extend the analytical modeling of the generation transients in moderate and strong inversions, one should note first that eqs. (1)-(4) are valid in all regions of inversion (weak, moderate and strong). Another key remark is that in moderate/strong inversions, Q_{inv} could no longer been neglected with respect with Q_d. The proposed modeling is based on a new unified expression for the inversion charge, similar to [3]:

$$Q_{inv}=\frac{\eta}{\beta}C_{ox}\ln\left\{\frac{\sqrt{2}}{2}\frac{\eta-1}{\eta}\exp\left(\frac{V_G-V_{FB}-2\eta\phi_F}{\eta/\beta}\right)+1\right\} \tag{10}$$

where η is the sub-threshold parameter. The model is limited to the linear region of operation (low V_D), where I_D is proportional to Q_{inv}. The new analytical equations, valid in all inversion regions, and similar to (6)-(9), are then deduced by replacing Q_{inv} given by expression (10) in eq. (2). The detailed investigations, based on the unified charge and current expressions, are given elsewhere [4].

4 2-D NUMERICALLY-BASED MODEL VALIDATION AND ACCURACY ANALYSIS

4.1 Simulation of weak inversion current transients induced by an opposite gate step-function

A systematic validation of the weak inversion transient compact model on both *elementary* and *realistic* long-channel (>10µm) structures has been carried out by 2-D numerical simulation with Atlas (Silvaco) [5]. Different generation parameters have been injected into Atlas and then fully confirmed by the proposed extraction methodology and modeling (Figs. 1 and 2).

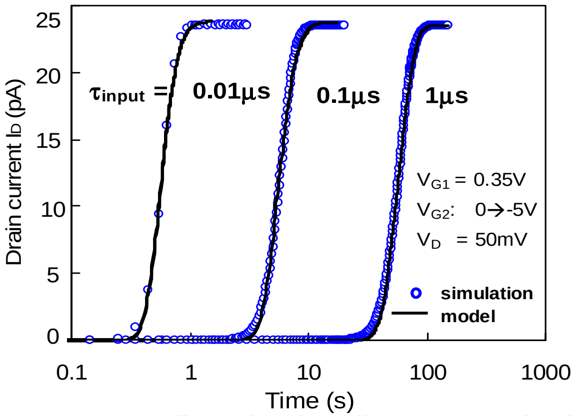

Fig. 1: Numerically- and analytically- (eq. 8) simulated drain current transients in weak inversion, for different carrier generation lifetime values.

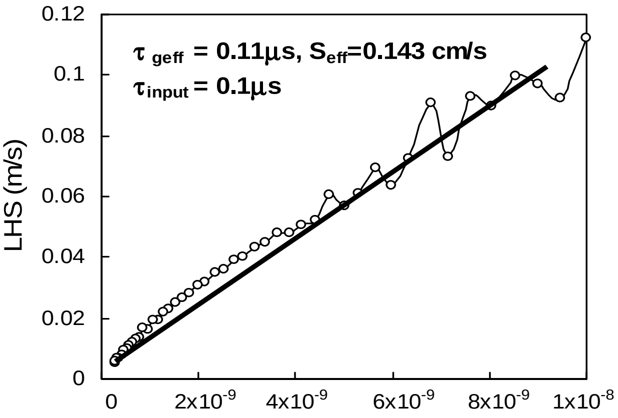

Fig. 2: τ_{geff} extraction linear plot based on the weak inversion model, eq. (7).

For example in Fig. 1, a fixed value, τ_{input}, was set and the drain current transient was calculated by both the 2-D simulator and our model (eq. 8). As shown in Fig. 1 for three different values of generation lifetime, our model perfectly fits the numerically simulated characteristics. Moreover, this validation procedure was applied to the extraction method: generation lifetime calculated using relation (7) from Atlas simulated transients matches very well the input values (Fig. 2 and Table 1). Our results demonstrate that the model shows excellent ability to track decades of lifetime and surface generation values, with errors less than 5%.

Input generation lifetime, τ_{input}	Extracted $(\tau_{geff})_{extr}$
1×10^{-8} s	0.96×10^{-8} s
1×10^{-7} s	1.1×10^{-7} s
1×10^{-6} s	1.08×10^{-6} s

Table 1: Extracted generation lifetime for different τ_{input}.

4.2 Weak inversion current transients induced by the front gate switch-off

Special concerns for analog SOI MOS switches (switched-data circuits) [6] and/or for SOI DRAMs [7] motivate the requirements in terms of accurate compact models for weak inversion transients in PD SOI MOSFETs. We demonstrate here that our model is able to fully describe the transient regime induced by switching the front gate from strong or moderate regime into weak inversion [6], as shown in Fig. 3. The physical mechanisms are identical and the same current transient expression (eq. 8) applies. Moreover, this specific transient regime can be originally used to tune the generation parameters without loss of accuracy.

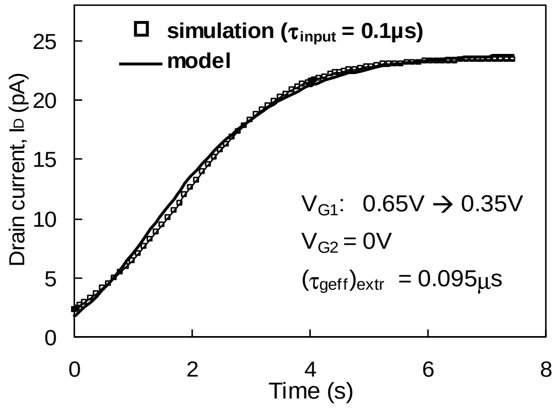

Fig. 3: Comparison between compact model and numerically data for a moderate to weak inversion front-gate-driven transient regime.

5 ADVANCED ULTRA-SHORT CHANNEL ANALYSIS

The model has been used to investigate weak inversion transients in down to 50nm SOI MOSFETs. In an advanced ultra-short channel transistor, the junction contribution to the generation process results in an equivalent reduction of transient duration, Fig. 4, which is reflected in a decrease by up to 80% of the effective extracted generation lifetime, τ_{geff} (Fig. 5). However, by including this generation contribution in the effective generation lifetime, the proposed model is still able to predict the transient behavior in 50nm channels with a relative error less than 10%.

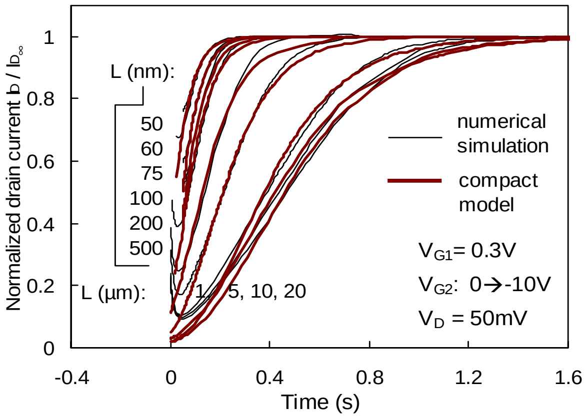

Fig. 4: Numerically-simulated drain current transients in weak inversion with the channel length as a parameter (realistic structure: SOI MOSFET 0.1µm).

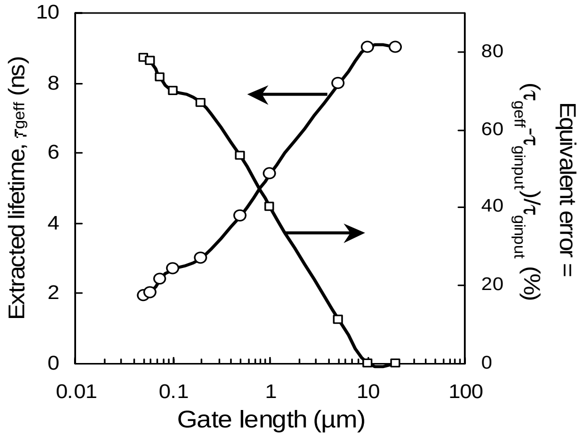

Fig. 5: Equivalent lifetime estimation error due to junction influence in ultra-short channels (realistic structure: SOI MOSFET 0.1µm).

Moreover, we were able to include via numerical simulation the effect of the interface generation velocity into the effective extracted lifetime. A simple relationship applies in Atlas [5]:

$$1/\tau_{geff} = 1/\tau_g + 2sL/A \qquad (11)$$

which can simply describe edge generation-recombination effects in unclosed transistor architectures (A is the gate area). Fig. 6 presents transients obtained for different injected s values. The impact on τ_{geff} is correctly estimated by our model, since $(\tau_{geff})_{extr}$ extracted by the model fits perfectly the theoretical value of τ_{geff} given by relation (11).

One key advantage of our model compared to the previous strong inversion analysis [8], is that *no knowledge* is required on the carrier mobility for the generation parameter extraction. In order to highlight this feature, we artificially forced different constant mobility values in Atlas, for a L_g=0.1µm realistic structure and then we extract τ_{geff}, which was found independent on the input carrier mobility. Table 2 demonstrates this remarkable result, which is very useful for ultra-advanced device architectures (with ultra-short channels and ultra-thin oxides).

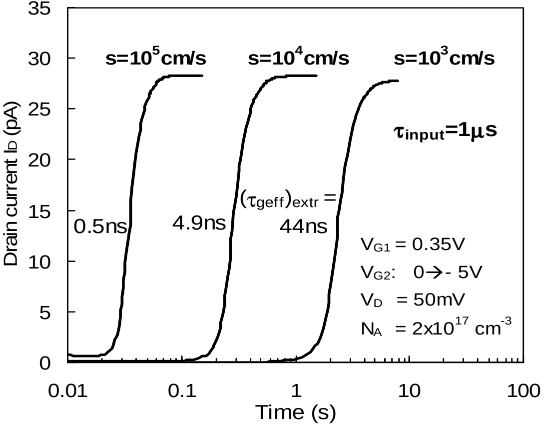

Fig. 6: Influence of the surface generation velocity on the numerically-simulated $I_D(t)$ and extracted τ_{geff} including s.

Input electron mobility	Extracted τ_{geff}
1000 cm^2/Vs	2.31 ns
700 cm^2/Vs	2.34 ns
500 cm^2/Vs	2.33 ns

Table 2: Extracted generation lifetime for different values of the channel mobility (L_g=0.1µm).

6 COMPACT MODEL PREDICTIONS

The proposed physical compact model naturally allows some extended predictions on the impact of transistor parameters on the related floating-body induced transient regimes. For the following investigations, the model has been priory calibrated on a real transient. Then: (i) the carrier lifetime, (ii) the surface generation velocity, (iii) the substrate doping and (iv) the oxide thickness were varied in realistic ranges and the subsequent weak inversion regime simulated.

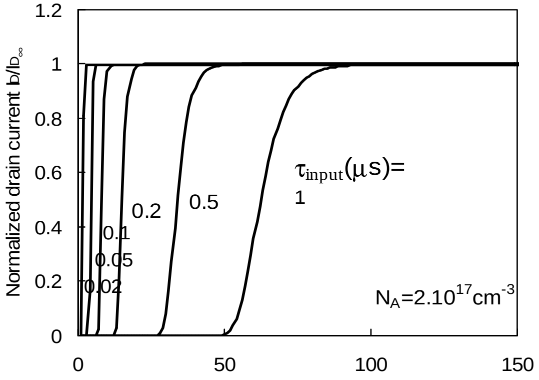

Fig. 7: Influence of the generation lifetime on the weak inversion transient behavior.

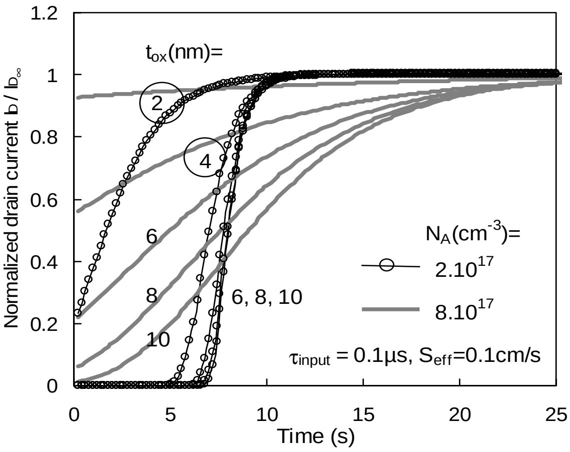

Fig. 8: Influence of t_{ox} on weak inversion transients.

Reduced lifetimes or increased S_{eff} values (or a combination of this) could result in important reduction of the generation weak inversion, as quantitatively suggested by Fig. 7. In Fig. 8 transient simulations suggest that with ultra-thin gate oxides PD SOI MOSFET, an increased front gate control suppress the current *off* duration but does not reduce the transient duration.

7 CONCLUSION

An original compact analytical model, which captures in its unique analytical expression main physical parameters, was proposed for the weak inversion transient regime of advanced PD SOI MOSFETs. The model accuracy and robustness have been validated by numerical simulation on submicron transistor architectures.

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