Modeling, Simulation and Comparative Analysis of RF Bipolar and MOS Low Noise Amplifiers for Determining Their Performance Dependence on Silicon Processing

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ABSTRACT

In this study, an investigation into MOS (metal-oxide semiconductor) and bipolar LNAs (Low Noise Amplifiers) in terms of their circuit design and the electrical circuit parameters was conducted. As partially reported [1], we have been methodically investigating physics base modeling and statistical simulations of the bipolar LNAs in terms of their associated semiconductor device, and silicon processing parameters. Here we report the comparative analyses of the single-stage, common source n-channel enhancement MOS transistor and common emitter class A npn bipolar LNAs. These 2.4 GHz low noise amplifier circuits were studied in terms of their electrical circuit parameters such as NF (Noise Figure) and output gain. Then, their dependence on semiconductor device, and silicon processing parameters for both technologies were compared and discussed in detail. A feasibility of implementing the novel statistical approach methodology was further investigated.

Keywords: Modeling, Simulation and Statistical Design of ICs, LNA in Wireless Communications, RF, Cost and Cycle Time Reduction in Semiconductor IC Manufacturing.

1 INTRODUCTION

The LNAs have been widely used in many applications including wireless personal communication systems [3-6]. These low noise amplifier circuits were characterized in terms of electrical circuit parameters such as noise figure (NF), and output gain, Table 1. The next step was to obtain the circuit equations for these parameters using the small signal model. The output gain A_v , for the bipolar and MOS LNA can be given by the Equations 1 and 2, respectively,

$$A_v = 20\log\left\{\sqrt{\frac{V_p\beta^3 V_t^3 C\pi I_{cc}^2 + V_p\beta^2 V_t^2 I_{cc}^3}{(I_{cc}V_t\beta + \beta I_{cc}^2 Ze + I_{cc}Ze\beta V_t C\pi + I_{cc}^2 Ze)(2V_t^2\beta C\pi + 2V_t I_{cc})^2}}\right\} \quad (1)$$

$$A_v = 20\log\left[\frac{\mu_n C_{ox} W (V_{GS} - V_t)\sqrt{\frac{R_d}{\varpi C_{gs}}}}{2L_{eff}}\right] \quad (2)$$

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	Circuit Simulation			*Electrical Goals*		
Parameter	*2.4 GHz*	*2.45 GHz*	*2.5 GHz*	*Min*	*Typ*	*Max*
Av (dB)	17.1	17	16.9	17	20	23
NF (dB)	4.6	4.6	4.6	-	2	3

Table 1: The SPICE circuit simulation data of three output electrical parameters over operation frequency at V_{cc} =2.7 V. The last three columns shows electrical goals over operation frequency and voltage.

Similarly, the noise figure (NF) has been derived for bipolar and MOS devices and was calculated to be for bipolar LNA,

$$NF = 10\log\left\{\frac{2\beta^2 I_{cc}V_t(|Z_y|)^2(R_{in} + r_b + RE) + (|Z_y|)^2(|Z_x|)^2 + 4R_{in}^2\beta I_{cc}^2(|Z_x|)^2}{2R_{in}\beta^2 V_t I_{cc}(|Z_y|)^2}\right\} \quad (3)$$

$$Z_y \_ 2R_{in}\beta V_t C_\pi + 2R_{in}I_{cc} + \beta V_t$$

$$Z_x \_ 2R_{in}\beta V_t C_\pi + 2R_{in}I_{cc} - \beta I_{cc}Z_e$$

and for the MOS LNA as

$$NF = 10\log\left(1 + \frac{2\gamma L_{eff}}{\mu_n C_{ox} W (V_{GS} - V_t) R_s Q_{in}^2}\right) \quad (4)$$

where the source resistance is given by

$$R_s = \frac{g_m L}{C_{gs}}$$

2 STATISTICAL MODELING AND SIMULATION METHODOLOGY

These electrical performance parameters presented Equations 1 through 4 and effects of silicon processing on these electrical goals of the both LNAs were separately investigated. Physics based mathematical models for the each circuit spec output parameter characterized and represented by semiconductor device and processing parameters. As a next step, micro-level semiconductor device models via MATLAB™ were created These physics-based device and process models were then coupled with unique

statistical simulation software called STADIUM [2] to create a robust circuit design which gives rise to a more compliant product with higher yields. STADIUM is a software program which couples computer simulators to a highly strong statistical method so called design of experiments.

The input parameters for the bipolar LNA device simulations are tabulated in Table 2. As for the statistical simulations, the long list of these input parameters in Table 2 have been screened via statistical simulations and then some semi empirical and random low and high values have been assigned to the highest contributor of seven input variables as shown in Table 2. Then these seven influential input variables have been used to run simulations using a statistical technique fractional factorial with resolution 3 over operation frequency and supply voltage. The factor contributions of these variables for each three output parameters along with mean and standard deviations have been calculated and compared to measurement values. The first selected seven input variables, doping concentration in base, doping concentration in emitter, collector-emitter voltage, emitter resistance, DC operating supply current, emitter width, and emitter and lead inductance as listed in Table 2 have been used to run multiple simulations.

Symbol	Input Parameter	Low	High
N_a (cm^{-3})	Doping concentration in Base	6E17	6.2E17
N_{dE}(cm^{-3})	Doping concentration in Emitter	3E18	3.2E18
V_{ce} (V)	CE voltage	0.9	1.0
I_{cc} (mA)	DC operating supply current	15.0	15.2
W_e (μm)	Emitter width	30	35
r_e (Ω.m)	Emitter resistance	25E-6	30E-6
L_e (H)	Emitter and lead inductance	1E-9	1.1E-9
V_{cc} (V)	Supply voltage	2.7 or 3.0 or 3.3	
f (GHz)	Operation frequency	2.4 or 2.45 or 2.5	
Q_B	Bulk charge	not varied	
T	Diffusion time	not varied	
T_d	Diffusion temperature	not varied	
D	Diffusion coefficient	not varied	
N_c	Doping concentration in Collector	not varied	
D_n & D_p	Diffusion constant for electrons & holes	empirically calculated	
τ_n (s)	Life time of electrons	2.5E-3	
τ_p (s)	Life time of holes	2.5E-3	
x_{jB}	The Collector-Base junction depth	0.433E-4	
x_{jE}	Emitter junction depth	0.316E-4	
C_{je}	Emitter-Base junction depletion cap	2.9E-9	
r_b	Transistor noise base resistance	616E-6 (Ω.m)/We	
T	Operation temperature	25 °C	

Table 2: Overview of input parameters for the bipolar LNA and their randomly selected low and high values for STADIUM statistical simulations.

Symbol	Input Parameter / Physical Constant	Low	High
C_{ox}	Gate Oxide Thickness, (F/cm^2)	3.8E-7	4.0E-7
L_{eff}	Effective Gate Length, (cm)	3.5E-5	3.7E-5
C_{gs}	Gate-Source Capacitance, (F)	6.7E-13	6.8E-13
R_s	Source Resistance, (_)	49	50
N_a	Substrate Doping Concentration, (cm^{-3})	6.0E17	6.2E17
W	Gate Width, (cm)	15.0E-3	15.2E-3
R_d	Drain Resistance, (_)	49	50
V_{GS}	The Gate-Source Applied Voltage, (V)	2.7 to 3.3	
f	Operation Frequency, (GHz)	2.4 to 2.5	
L_d	Gate Drawn Length, (cm)	0.6E-4	
V_t	Thermal Voltage, (V)	0.0259	
N_v	Effective Density of States in Valence Band, (cm^{-3})	1.04E19	
n_I	Intrinsic Carrier Concentration in Si, (cm^{-3})	1.5E10	
ε_o	The Permitivity of Free Space, (F/cm)	8.854E-14	
ε_r	Relative Dielectric Constant of SiO_2	3.9	
q	Electron Charge, (C)	1.602E-19	

Table 3: Overview of the MOS LNA input parameters and physical constants , their intuitively selected low and high values, and physical constants used in STADIUM statistical simulations.

Now, Table 3 summarizes the input parameters for the device performance parameters of the MOS LNAs. The seven input variables for the MOS LNA are the gate oxide thickness, the effective gate length, the gate-source capacitance, the source resistance, the substrate doping concentration, the gate width, and the drain resistance. These have been used to run multiple simulations using the same fractional factorial resolution III statistical DoE in STADIUM software, as was the case for the bipolar LNA [1]. After conducting several nominal value design of experiments, to make sure the location of the two chosen output responses, the seven input parameters as listed in Table 2 have been assigned variations. Using these assigned low and high values, two output responses were simultaneously simulated over operation frequency and supply voltage. Extraction of simulation data supplied necessary data for mean and standard deviation of each output response, and the individual

factor contributions for each input variables along with the prediction equation coefficients. Also, the factor contribution is a number which is used to determine the effect of the input variables on the variability of the each output response. Thus, the important factors to the output parameter can be easily attained by the factor contribution of each individual input.

3 ANALYSES AND RESULTS

The choice of circuits to demonstrate this new statistical approach is a 2.4 GHz bipolar low noise amplifier as described elsewhere [1]. This prototype single stage, common emitter, class A, npn high frequency low noise amplifier was built on a 0.6 µm BiCMOS Ultra High Frequency technology for mixed-signal RF applications with a f_t of 25 GHz.

The output gain simulation results for bipolar LNA displayed that the highest impacting input parameter was the doping concentration in emitter, n_{de} , as 65.53%. The remaining others from high to low were the doping concentration in base, n_a , and the collector emitter voltage V_{ce} nearly 15% each, the emitter inductance, l_e , 3.2%, the supply current, I_{cc} , 1.44% and almost negligible emitter resistance and width factor contribution. However, the noise figure simulations showed that the largest impacting input parameter was now the emitter width, W_e , rather than doping concentration in emitter, n_{de} , as was the case for the voltage gain. The factor contribution for the emitter width is 63.23 %. The other six parameters, high to low, were the emitter resistance, the doping concentrations in emitter and base, the DC operating supply current, the emitter inductance and the collector emitter voltage. It is noticeable that the cumulative sum of first two factors, the emitter width and resistance, contribution is greater than 91% which tells us that if circuit designer and process engineer pays attention to these parameters and related processing equipment, the NF performance can be easily optimized and become more robust which will lead to higher yields.

By the same token, the output gain simulation results for MOS LNA showed the highest impacting input parameter is the effective channel length, L_{eff} , with 71.84 %. The second highest one is the gate oxide thickness whose contribution is 20.28%. The remaining others from high to low were the gate width 4.08%, the drain resistance 2.37%, the gate-source capacitance 1.31%, the substrate doping concentration 0.12%, and almost negligible source resistance. Whereas the noise figure simulations displayed that the largest impacting input parameter is now the gate oxide capacitance, instead of the effective channel length which was the case for the output gain. The factor contribution for the gate oxide capacitance is 56.81% while the second largest impact comes from the effective channel length with only 27.49%. The other five parameters in descending order were the gate-source capacitance with 7.23%, the drain resistance with 3.65%, the substrate doping concentration with 2.82%, and the gate width with nearly 2% were the noticeably impacting inputs for the noise figure. On the other hand, influence of the drain resistance was almost negligible.

Furthermore, Figures 1 and 2 for the MOS LNA and Figures 3 and 4 for the bipolar LNA display the frequency dependence of electrical parameters. The mean and standard deviations of two output parameters of the hypothetical MOS LNA, the output gain and noise figure, have been calculated via statistical simulations over the operation frequency for the output gain and the noise figure. Several comparisons between both LNAs actual device measurements and also literature were made. The comparison of frequency dependence of both bipolar and MOS LNAs presented in Table 4.

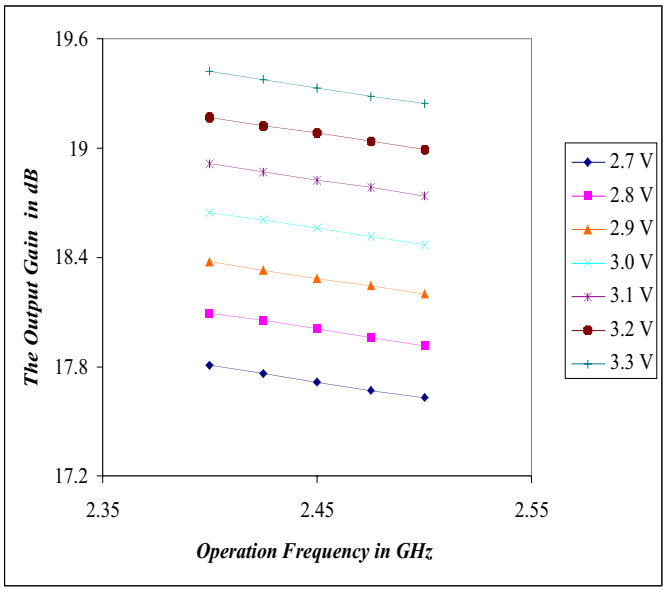

Figure 1: The statistically simulated output gain over the gate-source voltage versus the operation frequency for the MOS LNA.

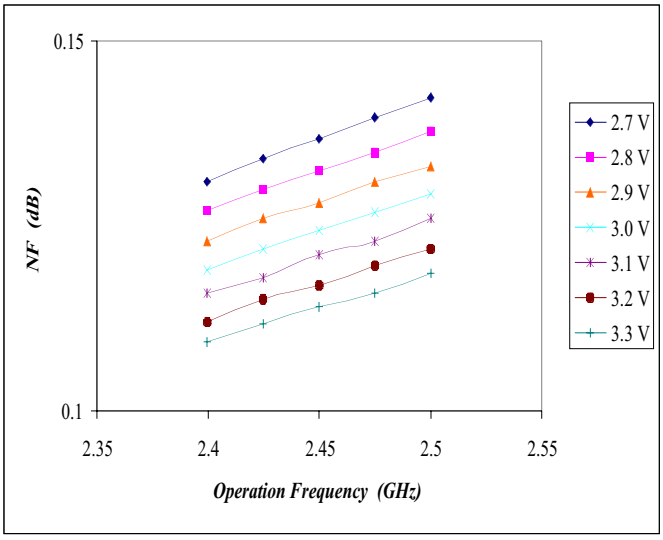

Figure 2. The statistically simulated noise figure over the gate-source voltage versus the operation frequency for the MOS LNA.

	MOS LNA Simulations			Bipolar LNA Simulations		
f (GHz.) / Param.	2.4 (_)	2.45 (_)	2.5 (_)	2.4 (_)	2.45 (_)	2.5 (_)
Av (dB)	18.65 (0.29)	18.56 (0.29)	18.47 (0.29)	15.84 (0.24)	15.75 (0.24)	15.66 (0.24)
NF (dB)	0.119 (.006)	0.124 (.007)	0.129 (.007)	3.79 (0.07)	3.79 (0.07)	3.79 (0.07)

Table 4: Comparison of the MOS LNA (at V_{GS} = 3.0 V) and Bipolar LNA (at V_{cc}=3.0V) statistical data of the mean values obtained from the statistical simulations for two final output electrical parameters over operation frequency.

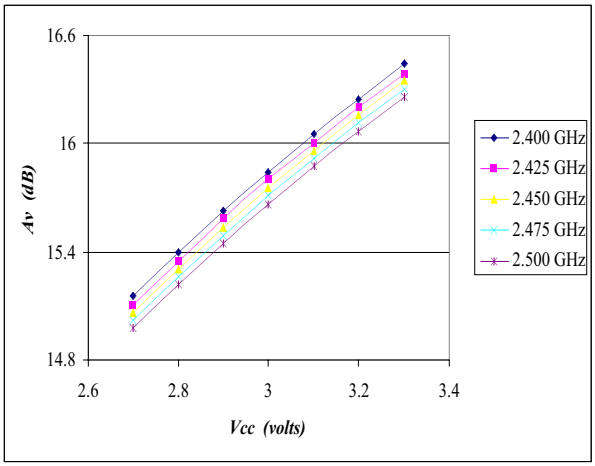

Figure 3: The output gain for bipolar LNA.

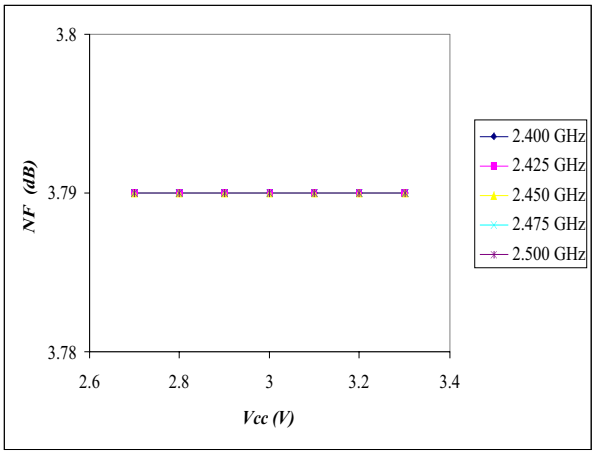

Figure 4: The noise figure for MOS LNA.

The output gain of the MOS LNA increases with the increasing supply voltage but the noise figure decreases with the supply voltage. These results are very much in agreement with literature and the similar results at lower voltages, 1V to 2V and at the lower operation frequencies, 1.49 GHz to 1.50 GHz have been reported [3-6]. No appreciable noise figure change and linear increase with the supply voltage for bipolar LNA were observed. As can be seen, the output gain in this hypothetical MOS LNA is 2.5 dB higher over the each supply voltage and the operation frequency range than that of the Bipolar LNA. Moreover, the significant noise figure reduction in the MOS LNA obtained throughout both the supply voltage and operation frequency ranges versus the Bipolar LNA.

Moreover, recall that the three most influential input factor contributions to the noise figure in the MOS LNA were the gate oxide capacitance, the effective gate length, and the gate width whereas for the Bipolar LNA case, these were the emitter width, the emitter resistance and the doping concentration in emitter. The striking analogy that the device geometry related the effective gate length in the MOS LNA and the emitter width in the Bipolar LNA play the same crucial role for determining device performance. It is also well known that the transition frequency f_t which is a measure of the maximum useful frequency of the transistor when it is used as an amplifier display very similar geometry dependence. In that case, the f_t of a bipolar transistor increases inversely with the square of the base width while the same frequency dependence for MOS transistor is inversely proportional to the square of channel length. Clearly, "the intrinsic device parameter f_t increases as the inverse square of the critical device dimension across which carriers are in transit" [6].

CONCLUSIONS

The novel statistical approach for analyzing and understanding associated manufacturing process parameters for the electrical circuit parameters was successfully implemented. An excellent agreement was observed between calculated results from this work and circuit simulation value of output gain which is within electrical goals. The noise figure and output gain are very good correlated with circuit simulation and measurement values. Thus, results of this analysis gives the statistical dependence of these output parameters on the semiconductor device and silicon processing parameters and leads to optimum solutions for the LNA circuit design and high volume manufacturing flow.

REFERENCES

[1] L.B Sipahi, B.A Myers, and T.J. Sanders, "A Method for Determining the Dependence of Integrated Circuit Performance on Silicon Process, Device and Circuit Parameters", *The Technical Proceedings of the Fourth International Conference on Modeling and Simulation of Microsystems*, pp.173-176, March, 2001.

[2] T.J. Sanders, K. Rekab, D.P. Means, and F. M. Rotella, "Integrated Circuit Design for Manufacturing through Statistical Simulation of Process Steps", *IEEE Trans. on Semiconductor Manufacturing*, November 1992.

[3] T.H Lee, *The Design of CMOS RF Integrated Circuits*, 1st Ed., Cambridge Univ. Press, p.272, 1998.

[4] R.G. Meyer, W.D. Mack, J.E.M. Hageraats, " A 2.5 GHz BiCMOS Transceiver for Wireless LAN's*", IEEE J. Solid State Circuits*, 32 (12), pp.2097-2104, 1997.

[5] J.C. Rudell, J.J. Ou, T.B.Cho, G. Chien, F. Brianti, J.A. Weldon, and P. Gray,., " A 1.9GHz Wide-Band IF Double Conversion CMOS Receiver for Cordless Telephone Applications", *ibid*., pp. 2071-2088, 1997.

[6] P.G. Gray, and R.G. Meyer, *Analysis and Design of Analog Integrated Circuits*, John Wiley & Sons Publishing Company, 1993.