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ABSTRACT

In this paper, we study the “non-quasi static” (NQS) behaviour of MOS transistors using an exact quasi static Look-up Table (LUT) [1] MOSFET model implemented in a general-purpose circuit simulator SEQUEL [2], device simulator ISE-TCAD [3] and SPICE BSIM3v3 [4] QS and NQS models. An NMOS transistor of channel length $2 \mu\text{m}$ is simulated using LUT, ISE and SPICE3 and terminal currents are qualitatively studied. The method for extraction of terminal charges, which are required for circuit simulation using the LUT approach also presented.

Keywords: Look-up Table, Non-Quasi-Static model, Terminal charges, MOSFET, circuit simulation.

1 INTRODUCTION

If the rise and fall times of the gate voltage of a MOSFET are comparable with the transit time, “non-quasi-static” (NQS) effects [5] become important. An accurate MOSFET circuit model must account for these effects. This is generally done by adding extra parameters and equations to an existing “quasi-static” (QS) model. This approach is acceptable if the QS model itself can be considered to correctly represent the device behaviour in all aspects except the NQS effects. In other words, in order to develop an accurate NQS model, it is necessary to validate or “calibrate” the QS model first. It is the purpose of this paper to present an accurate method to do this validation. In this method, device simulation is carried out first, and the currents and terminal charges so obtained are then used as “look-up” tables (LUT) to construct an “exact” QS model. This enables a qualitative comparison of the exact QS model with the BSIM3 QS model, and also that of device simulation results with the BSIM3 NQS model.

2 THE LUT APPROACH

In the QS approximation for MOSFETs, different terminal currents can be calculated as

$$I_x(t) = I_X(V_{BS}(t), V_{GS}(t), V_{DS}(t)) + \frac{dQ_X(V_{BS}(t), V_{GS}(t), V_{DS}(t))}{dt} \quad (1)$$

where X can be gate, drain, source, or substrate. In the look-up table method, the MOSFET is modeled as a table of DC currents I_D, I_G, I_B and terminal charges Q_B, Q_G, Q_D for the desired range of bias voltages, and then different terminal currents during circuit simulation are calculated as per Eq. 1 after interpolating the data. The data table can be generated using device simulator without any approximation; thus, it gives an “exact” QS model.

The current I_X in Eq. 1 can be obtained by DC simulation for the required range of bias voltages. The charge denoted by Q_X in Eq. 1 is much more subtle. It is not simply the terminal charge obtained with device simulator. To appreciate this point, consider particularly the bulk (or “body”) terminal of a MOS transistor. The device simulator will always produce a negligible value of Q_B since the electric field in the neutral region near the bulk contact is very small, producing a small $Q_B = \int E \cdot dS$. So, the use of Q_B computed by DC simulation for LUT quasi-static model, will always predict a vanishingly small $I_b(t)$, irrespective of bias voltages. This prediction is obviously incorrect: particularly when an applied voltage ramp takes the device from accumulation to inversion, a significant bulk current must flow. This shows that it is not possible to obtain terminal charges directly from DC results. In the following, a new method is demonstrated to compute the terminal charges from device simulation results, without any approximation.

Consider an NMOS transistor with $V_D = V_D^0, V_B = V_B^0, V_S = 0$. DC simulations for the device are performed for several values of V_G between V_{G1} and V_{G2} . Transient simulation is then performed with a ramp applied to the gate such that at $t = t_1, V_G = V_{G1}$, and at $t = t_2, V_G = V_{G2}$. During transient simulation, the gate voltage is varied, keeping other voltages fixed. All terminal currents are recorded as a function of time. Eq. 1 is now used to compute, for example, $\frac{dQ_G}{dt}$ as,

$$\frac{dQ_G(V_B^0, V_G(t), V_D^0)}{dt} = I_G(t) - I_G(V_B^0, V_G(t), V_D^0), \quad (2)$$

the right-hand side being exactly known from the simu-

lation results. Also,

$$\frac{dQ_G}{dt} = \frac{\partial Q_G}{\partial V_G} \frac{dV_G}{dt} = \frac{\partial Q_G}{\partial V_G} \left(\frac{V_{G2} - V_{G1}}{t_2 - t_1} \right) \quad (3)$$

From Eqs. 2 and 3, $\frac{\partial Q_G}{\partial V_G}$ is calculated, which is numerically integrated to obtain $Q_G(V_B^0, V_G, V_D^0)$, where $V_{G1} < V_G < V_{G2}$. The above calculation is repeated for other charges (Q_B, Q_D), and for several values of V_B^0, V_D^0 in the range of interest. The constants of integration involved in the numerical integration steps are assigned to ensure a consistent description of the charges. In this work, to construct the Look-up table for 2 μm channel length NMOS, we applied a gate voltage ramp with a rise time $\tau_r=1 \mu\text{sec}$ with different values of V_D^0 and V_B^0 . As an example, $I_b(t)$ is shown in Fig. 1 for various values of V_B , and the bulk charge extracted from this data is shown as a function of V_G in Fig. 2. The DC currents I_D, I_G, I_B and terminal charges Q_B, Q_G, Q_D extracted as described above, are used to form look-up tables. A device model based on the look-up tables (called henceforth as the LUT model) has been implemented in the circuit simulator SEQUEL [2]. For interpolation between points, techniques described in [1] have been employed.

3 NQS BEHAVIOUR

The LUT or the “exact QS” model was implemented using the interpolation schemes described in [1]. For device simulation, the ISE-TCAD package was used. For BSIM3 results, MOSIS model parameters were used, with some modifications. The ISE results are to be treated here as the “exact” NQS results and the LUT results as the “exact” QS results. Note that it would make sense here to compare *quantitatively* the ISE and LUT results with each other; also the BSIM3 QS and NQS results with each other, but not ISE/LUT results with the BSIM3 QS/NQS models, as the BSIM3 parameters used in this work have not been extracted for the simulated device. We will therefore undertake only a qualitative comparison in the following. Two transients are studied in the following: (i) the “ V_G transient” in which V_D, V_B, V_S are held constant and rising or falling edge with a given rise or fall time is applied to the gate. (ii) the “ V_D transient” in which a rising or falling edge is applied to the drain, the other terminals being held at a constant voltage. Note that, in the following, the results for the rising and falling edges have been plotted together in the same figure. The major conclusions that can be drawn from the simulation results shown in Figs. 4-12 are: (a) When V_D is held constant (4 V), and V_G is changed, the ISE and LUT results, which represents NQS and QS behaviour, respectively, show a substantial discrepancy (see Figs. 3, 4, and 5) owing to the NQS effects. The BSIM3 QS model compares well with the

exact QS (LUT) model (see Figs. 4 and 6) with 40/60 partitioning, but not with 0/100 partitioning. Comparison of the BSIM3 NQS results (Fig. 7) with the exact NQS (ISE) results (Fig. 4) shows that the BSIM3 NQS model predicts an unexpected trend for the rising V_G edge, viz., I_d continues to decrease even after the initial drop. By decreasing the `elm` parameter of the BSIM3 NQS model, it is possible to dampen this effect; however, it results in an unreasonably long “tail” after V_G has reached 4 V. (b) When V_G is held constant (4 V), and V_D is changed, the terminal currents (see Figs. 8, 9, and 10) as obtained with the ISE and LUT are almost the same. BSIM3 QS model shows a behaviour which is qualitatively very different from the exact QS (LUT) model. On the other hand, the NQS model does show trends that are qualitatively similar to the exact NQS results. (c) In the V_G transient, the BSIM3v3 NQS model predicted zero bulk current, whereas, in the V_D transient, it predicted a finite bulk current (not shown) which was qualitatively similar to the exact NQS (i.e., ISE) result. This discrepancy in the BSIM3v3 NQS results needs to be investigated further.

4 CONCLUSIONS

NQS behaviour in MOS transistor using the LUT approach has been studied. The exact QS and NQS results were compared qualitatively with SPICE QS and NQS models. The results presented here already point to the fact that the BSIM3v3 QS and NQS models may both need to be improved to correctly account for the NQS behaviour of a MOSFET.

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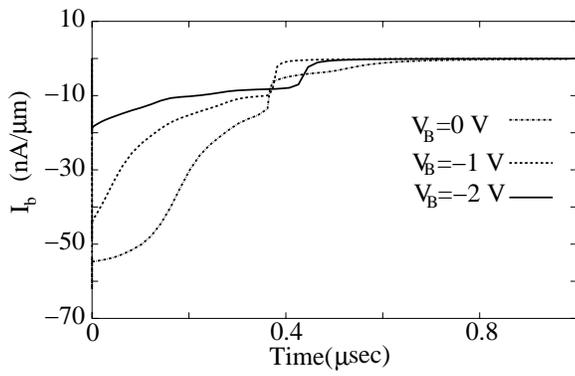


Figure 1: Bulk current, as obtained with ISE, as a function of time for different values of V_B , when V_G is varied from -2 V at $t=0$ to 5 V at $t=1 \mu\text{sec}$ ($V_D=1 \text{ V}$).

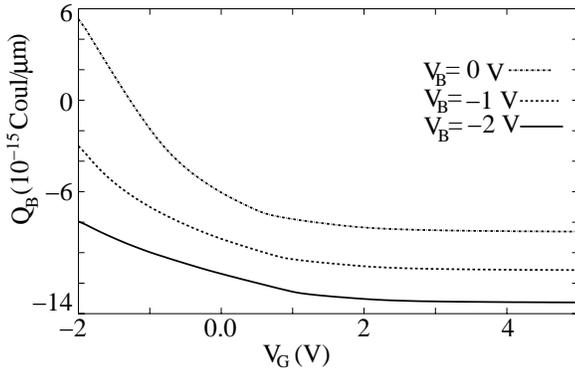


Figure 2: Bulk terminal charge computed from the results shown in Fig. 1.

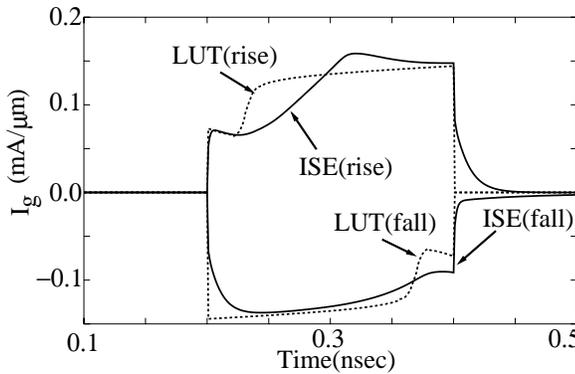


Figure 3: ISE and LUT simulated gate current; $V_D=4 \text{ V}$, $V_B=V_S=0.0 \text{ V}$, and V_G is 0 V (4 V) at $t=0.2 \text{ nsec}$, reaches 4 V (0 V) at $t=0.4 \text{ nsec}$.

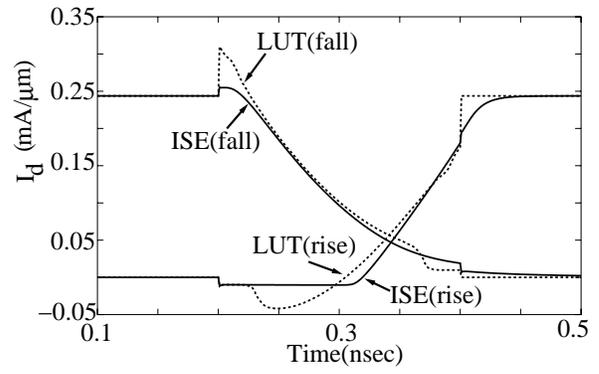


Figure 4: ISE and LUT simulated drain current; $V_D=4 \text{ V}$, $V_B=V_S=0.0 \text{ V}$, and V_G is 0 V (4 V) at $t=0.2 \text{ nsec}$, reaches 4 V (0 V) at $t=0.4 \text{ nsec}$.

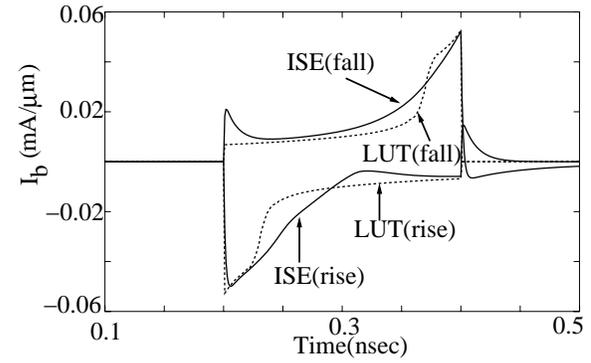


Figure 5: ISE and LUT simulated bulk current; $V_D=4 \text{ V}$, $V_B=V_S=0.0 \text{ V}$, and V_G is 0 V (4 V) at $t=0.2 \text{ nsec}$, reaches 4 V (0 V) at $t=0.4 \text{ nsec}$.

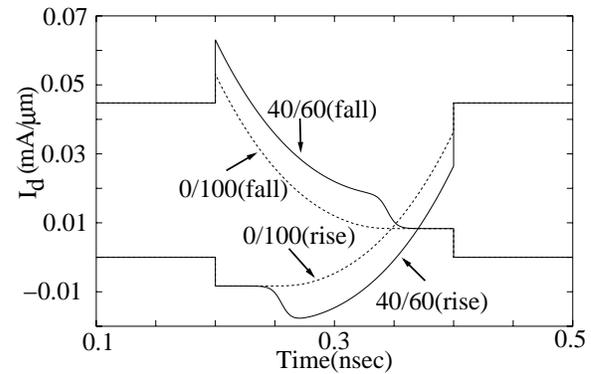


Figure 6: SPICE3 BSIM3v3 QS simulated drain current with charge partitioning schemes 40/60 and 0/100; $V_D=4 \text{ V}$, $V_B=V_S=0.0 \text{ V}$, and V_G is 0 V (4 V) at $t=0.2 \text{ nsec}$, reaches 4 V (0 V) at $t=0.4 \text{ nsec}$.

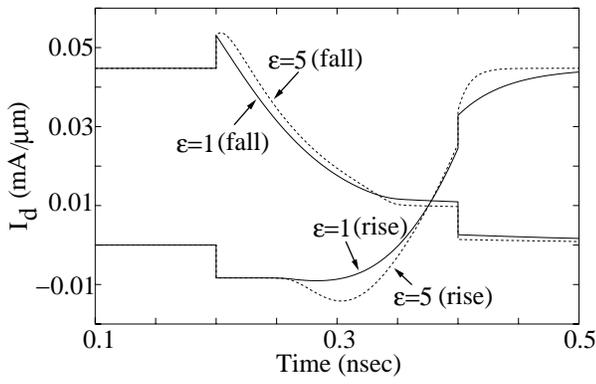


Figure 7: SPICE3 BSIM3v3 NQS simulated drain current with **elm** 1 and 5; $V_D=4$ V, $V_B=V_S=0.0$ V, and V_G is 0 V (4 V) at $t=0.2$ nsec, reaches 4 V (0 V) at $t=0.4$ nsec.

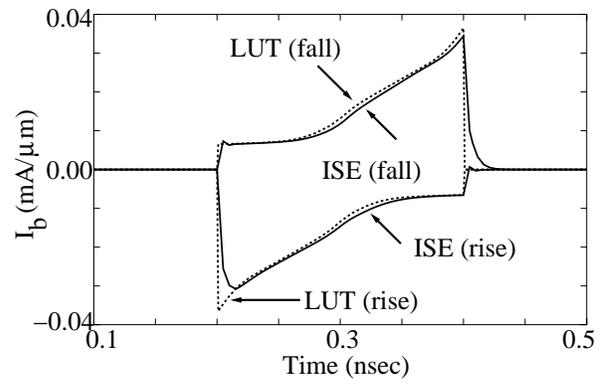


Figure 10: ISE and LUT simulated bulk current; $V_G=4$ V, $V_B=V_S=0.0$ V, and V_D is 0 V (4 V) at $t=0.2$ nsec, reaches 4 V (0 V) at $t=0.4$ nsec.

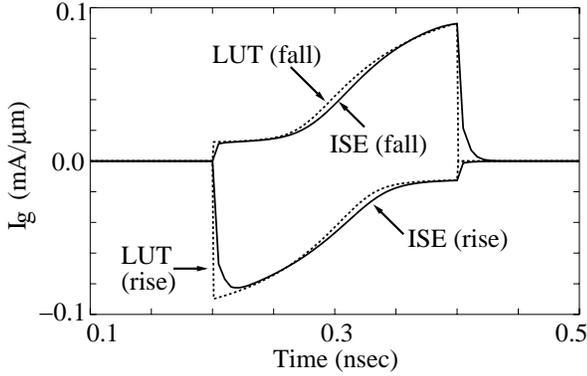


Figure 8: ISE and LUT simulated gate current; $V_G=4$ V, $V_B=V_S=0.0$ V, and V_D is 0 V (4 V) at $t=0.2$ nsec, reaches 4 V (0 V) at $t=0.4$ nsec.

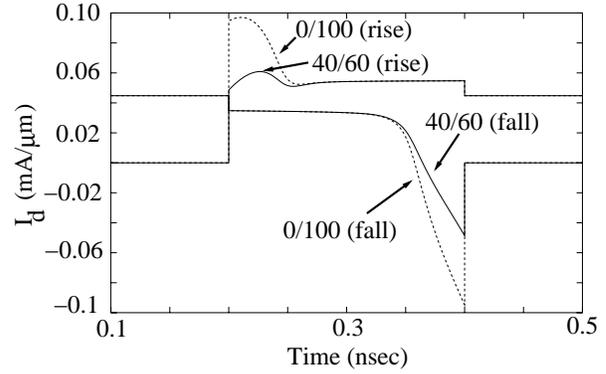


Figure 11: SPICE3 BSIM3v3 QS simulated drain current with charge partitioning schemes 40/60 and 0/100; $V_G=4$ V, $V_B=V_S=0.0$ V, and V_D is 0 V (4 V) at $t=0.2$ nsec, reaches 4 V (0 V) at $t=0.4$ nsec.

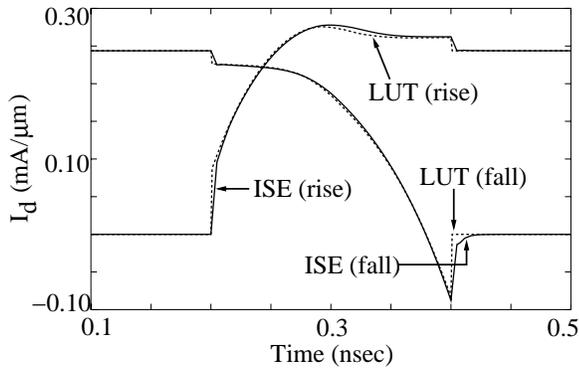


Figure 9: ISE and LUT simulated drain current; $V_G=4$ V, $V_B=V_S=0.0$ V, and V_D is 0 V (4 V) at $t=0.2$ nsec, reaches 4 V (0 V) at $t=0.4$ nsec.

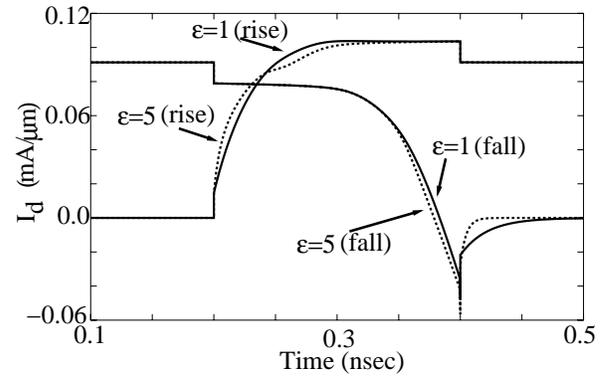


Figure 12: SPICE3 BSIM3v3 NQS simulated drain current with **elm** 1 and 5; $V_G=4$ V, $V_B=V_S=0.0$ V, and V_D is 0 V (4 V) at $t=0.2$ nsec, reaches 4 V (0 V) at $t=0.4$ nsec.