# A New Analytical Model of Channel Hot Electron (CHE) and CHannel Initiated Secondary ELectron (CHISEL) Current Suitable for Compact Modeling

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## ABSTRACT

This paper presents for the first time a new approach to hot-carrier phenomena leading to an analytical model of both Channel Hot Electron (CHE) and CHannel Initiated Secondary ELectron (CHISEL) currents. This model can be incorporated in Spice-like models of MOS transistors and Floating Gate (FG) devices to include hot carrier phenomena also in circuit simulations.

**Keywords:** compact modeling, semiconductor device modeling, hot carrier effects, MOSFET, Flash memory.

## 1 INTRODUCTION

Interest in studying CHE current has grown in the last years for two reasons: i) its negative effects on the MOS reliability, related to the generation of interface states and charge in the oxide above the drain junction; ii) it is the most used mechanism for programming Flash memories.

More recently, a new program mechanism, namely the CHISEL injection, has been introduced in Flash memories to overcome the major disadvantages of CHE injection [1]. However, up to now CHISEL current simulations required Monte-Carlo calculations to model the high energy tail of electron energy distributions, but this is computationally very expensive, thus discouraging a frequent use [1].

In this scenario, the goal of this work has been the development of a new analytical model of gate current in MOS transistors including both CHE and CHISEL contributions. In this process, the real capability of an analytical model to describe such complex physical phenomena will be critically reviewed.

## 2 THE MODEL

Since this model is designed to be incorporated in compact models of MOS [2] or FG devices [3], in the following we will suppose to know from the Spice-like model adopted: the drain-source current, $I_{DS}$, the saturation voltage, $V_{SAT}$, and the length of the pinchoff region, $\Delta L_E$.

For clarity, we will split the description of the model in two parts: i) the calculation of the CHE current; ii) the new analytical model of the CHISEL current.

For a correct modeling of hot-carriers phenomena, an accurate estimate of the electric field in the channel is required. The peak value of the lateral field has been calculated approximating its shape in the pinchoff region with a triangular one: $E_M=2(V_{DS}-V_{SAT})/\Delta L_E$. The lateral field, which grows almost exponentially going from source to drain, is given by $E_P=E_{MIN}\cdot\cosh(x/L)$, where $E_{MIN}$ is the minimum channel field, and L is a constant parameters [4]. Then, we have calculated the potential along the channel, $V_C$, the oxide field, $F_{OX}$, and the field in the silicon normal to the channel.

### 2.1 The CHE current calculation

The modeling of CHE current, $I_{CHE}$, has been addressed following the approach proposed in [5].

Schematically, to contribute to gate current hot electrons must have kinetic energy higher than the $Si/SiO_2$ barrier (to be able to overcome it) and velocity direction toward the gate (to be collected at the gate). Therefore, to calculate $I_{CHE}$, the electron energy and momentum distribution, and the probability to cross the oxide barrier have to be determined.

For the electron energy distribution, we adopted the analytical model used in [6], which takes into account the non-Maxwellian form of its high energy tail: $f_{el}(E,E_P)=K\cdot\exp(-\chi E^3/E_P^{1.5})$, where K and $\chi$ ($=1.3\cdot10^8$ $V^{1.5}cm^{-1.5}eV^{-3}$) are two constant parameters.

The momentum distribution has been considered almost spherical, being the momentum relaxation time constant much smaller than the energy relaxation time constant [5].

The probability of an electron to cross the oxide barrier is given by the product of a) the tunneling probability, $P_{TUN}$, calculated by the WKB method, which takes into account the charge quantization and the increase of the potential barrier due to the reverse oxide field; b) the probability that the electron velocity is directed toward the gate, $P_V=\vartheta/4\pi$, where $\vartheta$ is the spatial angle in the momentum space directed toward the gate; c) the probability that electrons do not loose energy when traveling the distance to the interface, $P_C=\exp(-d/\lambda)$, where d is the distance from the re-direction point to the $Si/SiO_2$ interface, and $\lambda$ is the electron mean free path [5].

The CHE current is given by (1), where $L_E$ is the effective channel length of the device.

$$I_{CHE} = I_{DS}\int_0^{L_E}\int_0^{\infty} f_{el}[E,x]\cdot P_{TUN}[E,x]\cdot P_V P_C\cdot dE\cdot dx \qquad (1)$$

## 2.2 The CHISEL current

The CHISEL current can be modeled following the same theoretical approach, provided that accurate expressions for carrier Energy Distributions (**ED**) are derived.

This complex task is usually addressed through Monte Carlo simulations [1], as electrons involved in CHISEL mechanism are generated through the following four physical mechanisms. Schematically: hot channel electrons, e1, ionize into the drain producing electron-hole pairs (e2-h2) with multiplication factor $M_1$ (**1st M**echanism: Impact Ionization, **II**). e2 are collected at the drain, whereas h2 are heated by the high field at the drain junction (**2nd M**: Energy Gain, **EG**), and ionize again with multiplication factor $M_2$ (**3rd M**: **II**). Thus, new electron-hole pairs (e3-h3) are generated: electrons e3 are driven toward the $Si/SiO_2$ interface (**4th M**: **EG**), reaching it where the oxide field is more favorable to cross the barrier, whereas h3 holes are collected at the body.

The core of this model is given by the new approach adopted to calculate analytically the e3 **ED** from the e1 one. It is based on two functions, called Transformation Functions, **TFs**, that model **ED** changes induced by each one of these four mechanisms, as it will be illustrated in the following.

The first **TF** models the **ED** of carriers generated by **II** (secondary) as a function of the **ED** of primary carriers. To build this function, we have to consider that the primary carrier with energy E loses a part of its energy, $E_G$, to form a new electron-hole pair, and the remaining energy, $E\text{-}E_G$, is redistributed among the primary carrier itself and the new electron-hole pair. Thus, the average energy of secondary carriers is $E_{MED}=(E\text{-}E_G)/3$ [1], while their maximum, $E_{MAX}$, and minimum, $E_{MIN}$, are $E\text{-}E_G$ and zero, respectively. Since the probability for a carrier to have both $E_{MAX}$ and $E_{MIN}$ energy is negligible, **TF** is zero at those points. Moreover, it must have its mean value at $(E\text{-}E_G)/3$, and its integral is equal to unity. With all these constraints, we chose for the first **TF** a beta distribution function.

The second **TF** models ED changes of carriers which have gained energy from the electric field at the drain-body junction (2nd and 4th **M**). The maximum energy a carrier can gain (if ideally it does not suffer any collision), $\Delta E_{MAX}$, can be easily estimated from the potential profile. Its average energy, $\Delta E_{MED}$, can be calculated from (2), which accounts in a simple way for the first order non-local effects, neglecting generation-recombination and heat flux [7].

$$\Delta E_{MED}(x)=\frac{3}{5}\int_0^x q\cdot F(\xi)\cdot\exp\left(-\frac{x-\xi}{\lambda_\omega}\right)d\xi \qquad (2)$$

$\lambda_\omega$ is the energy relaxation length and F is the field along the path followed by carriers. Then, the 2nd **TF** is zero at E=0 and $E=\Delta E_{MAX}$; it has the mean at $E=\Delta E_{MED}$ and its integral is equal to unity. To satisfy all these constraints, a beta distribution function has been chosen also as the **TF** for the energy gain.

The e3 energy distribution, $f_{e3}(E)$, is determined from $f_{e1}(E)$ by applying in series the **TF** corresponding to the four mechanisms above described.

1) The h2 **ED** is calculated from the e1 one through (3), that is: the amount of holes h2 with energy E generated by **II** is given by the sum of all primary e1 electrons with energy $E^I>E+E_G$, multiplied by the probability that they really ionize transferring the energy $E^I-E$ to the newly generated h2 holes.

$$f_{h2}(E)=\int_{E+E_G}^{\infty} M_1\cdot f_{e1}[E'+E_G,E_P]\cdot f_{TF,I}\left(\frac{E}{E'+E_G}\right)\cdot dE' \qquad (3)$$

2) The **ED** of *energetic* h2 holes (those that gained energy from the high field at the drain/body junction until they ionize) has been evaluated through (4), that is: the amount of *energetic* holes with energy E is the sum of all the *cold* holes (those just generated by **II**) with energy $E^I<E$, multiplied by the probability that they gain the energy $E-E^I$ traveling toward the body.

$$f_{h2,E}(E)=\int_{E-\Delta E_{MAX}}^{E} f_{h2}(E')\cdot f_{TF,2}\left(\frac{E-E'}{\Delta E_{MAX}}\right)\cdot dE' \qquad (4)$$

$\Delta E_{MAX}$ has been estimated from the potential profile, $V_C$. $\Delta E_{MED}$ has been calculated summing contributions due to both the lateral and the normal field in the silicon, that have been separately evaluated by applying (2). To calculate the integral range in (2), we determined the h2 ionization point evaluating the trajectory of h2 and equating the distance traveled by h2 holes to the energy relaxation length.

The e3 electron population at the $Si/SiO_2$ interface results from the *energetic* h2 one through the **II** (**M3**) and the next **EG** of the just generated e3 electrons (**M4**). Hence, their **ED** can be derived from $f_{h2,E}$ following the same procedure adopted for the first two mechanisms.

Then, CHISEL current can be calculated through

$$I_{CHISEL}=I_{DS}\int_0^{\infty} f_{e3}(E)\cdot P_{TUN}(E)\cdot dE \qquad (5).$$

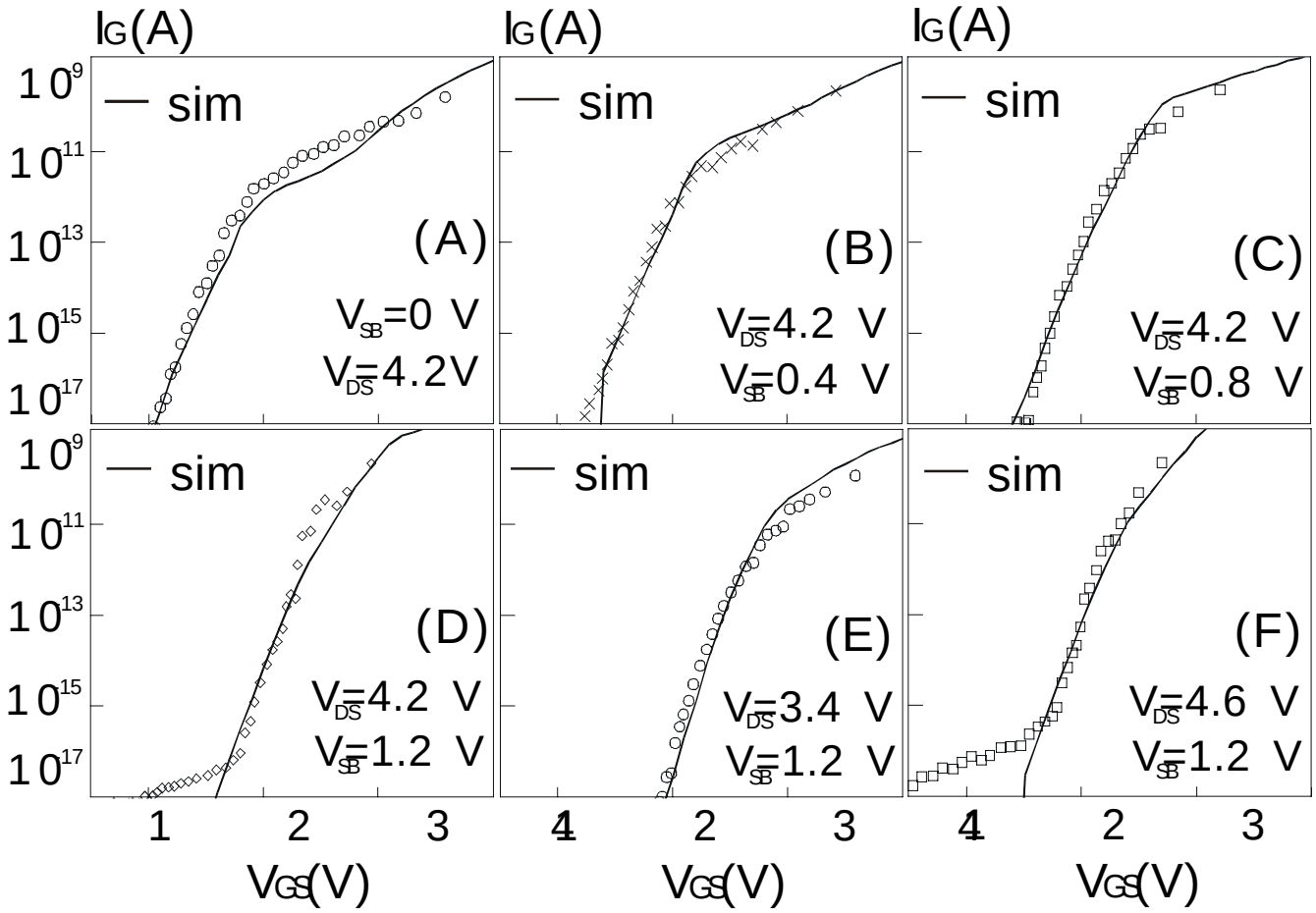


Figure 1. CHE-CHISEL currents simulated by our model (solid lines) and measured on an equivalent MOS (symbols) as explained in [5] applying different body and drain voltages (W=0.16 μm, L=0.3 μm).

## 3 SIMULATION RESULTS

To test the actual capability of this model to reproduce real gate current characteristics, we simulated CHE and CHISEL current derived from threshold voltage measurements performed on 0.25 μm state-of-the-art Flash memory cell manufactured by STMicroelectronics. As the gate current, $I_G$, induced by CHE and CHISEL mechanisms is very small, its direct measurement is very inaccurate and it degrades heavily the device because of times involved. For this reason, $I_G$ is usually measured in a Floating Gate (FG) device with an indirect technique, based on the relation $I_G=C_{CG}\cdot dV_T/dt$ [5], where $C_{CG}$ is the capacitance between control and floating gates, and $V_T$ is the threshold voltage.

We calculated the FG potential, $V_{FG}$, of the Flash memory, which corresponds to the gate voltage, $V_{GS}$, of the simulated MOS transistor, by means of the compact FG memory model proposed in [3].

Regardless the many approximations taken in the CHE-CHISEL current model proposed, the accuracy of results is excellent, even though not comparable to that of MC techniques and device simulators. Particularly, as shown in Figs.1(a)-(f), the gate current simulated by this model agrees nicely with experimental data, reproducing correctly its increase due to both the negative biasing of the body [1], and to $V_{DS}$ reduction. Minor discrepancies can be due to the many approximations taken to model analytically the hot carrier physical phenomena, but this does not diminish the validity of the model in circuit simulations, where the accuracy of device simulations is not needed.

Schematically, approximations can be grouped in three major categories: 1) detailed physical and geometrical features of the devices (the shape of the drain junction, the substrate doping profile, the non uniformity of the tunnel oxide thickness, … ) are not considered, being the model devoted for Spice applications. 2) The inputs of this model, i.e. $I_{DS}$, $V_{SAT}$, and $\Delta L_E$, are known from compact models, hence they may be not accurate enough. In fact, parameters of Spice-like models are usually extracted at low biases, and therefore, when they are used in medium-high voltage conditions typical of program operations, they can lead to incorrect estimates of $I_{DS}$, $V_{SAT}$, and $\Delta L_E$. 3) The analytical nature of the model forces some approximations in the

calculation of: a) the field and the potential drop in the channel; b) the h2 hole ionization point, which is performed in mean, neglecting statistic tails of the physical phenomenon; c) the e3 energy distribution, which is evaluated by the new **TF** approach.

Since the **TF** approach is the core of this new way to handle analytically hot carrier phenomena, we evaluated carefully its sensitivity to the **TF** beta function shape. As expected, narrowing the **TF** change function (i.e. increasing beta function parameters), the high energy tail of e3 electron **ED** is strongly underestimated, and therefore, a large reduction occurs in the simulated CHISEL current (the e3 population which can overcome the oxide barrier decreases significantly). Although the dependence of the CHISEL current on the **TF** shape is significant, it can be fully compensated by an appropriate choice of K (a parameter of the e1 **ED**), which represents the only fitting parameter of this model and can be calibrated to obtain a good fitting of experimental current curves. Note that this calibrated value of K must be kept constant, since it depends strictly only on the **ED** beta function adopted, although minor influence of the Spice model adopted could be also expected.

Finally, we tested this CHE and CHISEL current model also incorporating it in the compact model of FG memories reported in [3]. To simulate accurately program operations of Flash memories, a voltage controlled current source implementing the CHE-CHISEL gate current has been added to the basic structure of the FG memory model. Fig. 2 shows simulations and measurements of the $V_T$ shift occurring during the program of the Flash cell, performed by applying to the control gate the voltage ramp plotted in the inset of Fig. 2, and varying the body voltage in the range 0/-1.5V. As shown in this figure, measured $V_T$ curves are excellently reproduced by the model, and particularly, the rise of the $V_T$-time curves on increasing $V_{SB}$ are correctly fitted without any additional parameter to improve the simulation quality.

## 4 CONCLUSIONS

In this paper, we presented for the first time a new analytical model of gate current including both Channel Hot Electron (CHE) and CHannel Initiated Secondary ELectron (CHISEL) injection mechanisms. This model, developed for Spice-like environments, has been demonstrated to be capable to simulate correctly CHE-CHISEL gate currents, thus including the effects of these physical phenomena in circuit simulators.

Although the accuracy of results on a single device cannot be compared to MC techniques and device simulators, this model demonstrates that the analytical approach can be adopted to handle effectively hot carrier physical phenomena in circuits, provided that a very detailed picture is not required.

Moreover, this model gives the possibility to simulate easily CHE and CHISEL currents without going to Monte-Carlo techniques, thus promoting the understanding of hot carrier related phenomena also in circuit simulations.

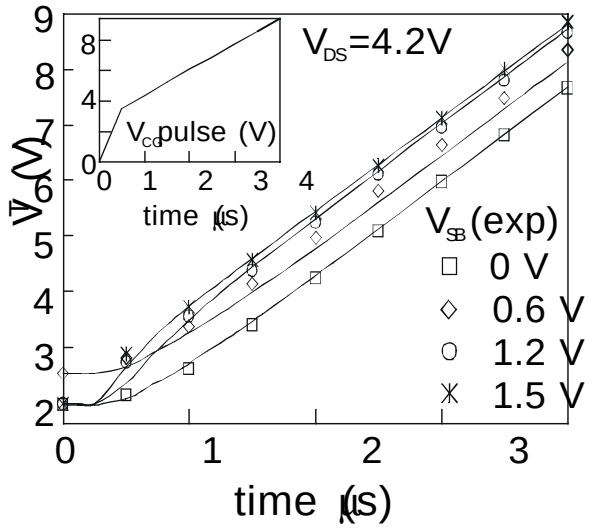


Figure 2. $V_T$ shift simulated incorporating the CHE-CHISEL model in [3] and measured during the program of a Flash memory.

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