Fail pattern classification and analysis system of memory fail bit maps

Koji Nakamae, Atsushi Itoh, Hiromu Fujioka

Department of Information Systems Engineering, Graduate School of Engineering
Osaka University, 2-1 Yamada-Oka, Suita, Osaka, 565-0871 Japan
{nakamae, itoh, fujioka}@ise.eng.osaka-u.ac.jp

ABSTRACT

In order to determine problematic wafer processing steps rapidly during memory production, the system that classifies failure patterns from memory fail bit maps (FBMs) and estimates the cause of failure is proposed. The system mainly consists of three procedures, the macro level failure pattern classification, the micro level failure pattern classification and the cause estimation based on the comparison of two level classified results with the expert knowledge. In the macro and micro levels, the failure patterns are classified into five and eleven categories, respectively. The system was applied to fail bit map data from recent DRAM devices to show its validity.

Keywords: memory fail bit map, fail pattern classification, cause estimation, expert knowledge

1 INTRODUCTION

Over the years, memory fail bit maps (FBM) have become an important diagnosis tool for testing memory devices. The predominant failure modes of a memory device could quickly be discovered by their characteristic fail patterns on a map. However, as memory devices become denser, it is very difficult to analyze fail bit maps and to estimate the cause.

Furthermore, as a result of cutthroat price competition in semiconductor manufacturing, manufacturing management problems to improve a manufacturing efficiency and to reduce the price have received considerable attention. Thus, it is urgently necessary to estimate problematic wafer processing steps or production equipment rapidly.

A pattern recognition algorithm suitable for efficient analysis of FBM has been reported [1]. The method enables an engineer to discover the primary failure modes of a memory device over a large population. The statistical analysis method for FBM has been reported [2]. However, these methods do not lead to the cause estimation.

In order to determine problematic wafer processing steps rapidly during mass production, the automatic memory failure analysis using an expert system with a memory tester [3] and the system that utilizes the computers between a conventional memory tester and a yield management database system [4] has been proposed.

In this paper, we propose a fail pattern classification and analysis system of memory FBMs when the computer directly linked with the memory tester is not used. The system can classify failure patterns from FBM and estimates the causes of failure in the wafer processing steps rapidly.

2 OUTLINE OF PROPOSED SYSTEM

The system mainly consists of three procedures, the macro level fail pattern classification, the micro level fail pattern classification and the cause estimation based on the comparison of two level classified results with the expert knowledge as shown in Fig. 1. Macro and micro levels mean wafer size and die size levels, respectively. In the micro level, a black pixel in the micro-level FBM corresponds to a failed memory bit cell. A black pixel in the macro-level FBM means that the area of 256 bits x 128 bits includes at least a failed memory bit cell in the micro level.

In the macro and micro levels, the fail patterns are classified into five and eleven categories, respectively according to the expert knowledge as shown in Table 1. Table 1 shows an example of the correspondence between failure phenomena (macro-level failure patterns) and the failed wafer processing steps (micro-level failure patterns). The structure in die is shown in Fig. 2.

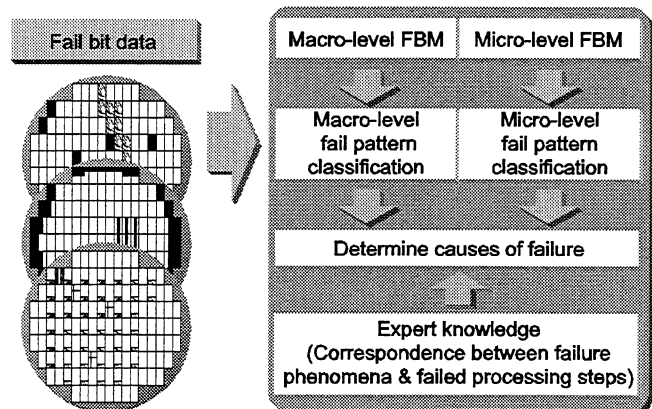

Figure 1: Outline of fail pattern classification and analysis system of FBM.

Table 1: Example of the correspondence between failure phenomena (macro-level failure patterns) and the failed wafer processing steps (micro-level failure patterns).

Micro level \ Macro level	Failed processing step \ Failure phenomena	Inside of single die on outer region	Inside of single die on central region	Across multiple dies on outer region	Across multiple dies on central region	Scratch
		A	B	C	D	E
Cross fail	Upper wire					
Block width word line fail	Upper wire					
Block width bit line fail	Upper wire					
Word line fail across two sub blocks	Lower wire (driver)					
Bit line fail across two sub blocks	Lower wire (sense amp)					
Word line fail in a sub block	Gate formation					
Bit line fail in a sub block	Bit line formation					
8-connected two bits fail with an address constraint	Bit line contact formation					
8-connected two bits fail with no address constraint	Channel stopper formation / Capacitor formation					
Single bit fail	Channel stopper formation / gate formation / capacitor formation					

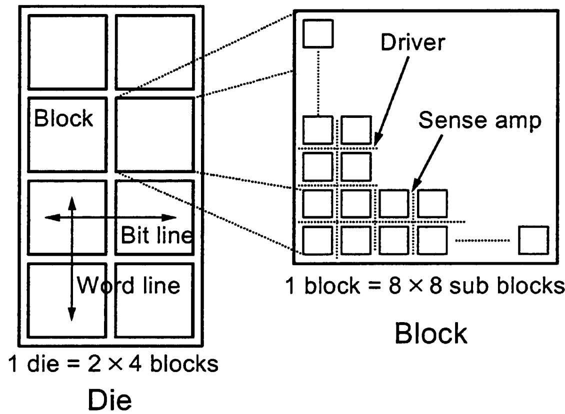

Figure 2: Die structure.

This table is made on the clear understanding of a cause-and-effect relationship between failed processing steps and failure phenomena. The table allows us to determine the causes of failure rapidly. A gray area in the table shows unknown causes of failure.

3 MICRO LEVEL FAIL PATTERN CLASSIFICATION

In the micro level fail pattern classification, failure patterns are searched in each memory block of die. Micro level fail patterns to be processed are treated in this study as shown in Table 1 where a category Mic11 "others" described later is omitted.

3.1 Micro level fail bit patterns

We classify micro level fail bit patterns into 11 categories by considering the correlation between the manufacturing steps and the fail bit patterns. Each pattern is defined as follows.

Category Mic1:"single bit fail pattern" means a fail bit that has no neighboring fail bits in the square of several bits. The estimated cause step is the channel stopper formation, the gate formation, or the capacitor formation.

Category Mic2:"8-connected two bits fail with no address constraint" means that two fail bits are connected in the 8-connectivity and these two fail bits are not controlled by one single bit line. The estimated cause step is the channel stopper formation or the capacitor formation.

Category Mic3:"8-connected two bits fail with an address constraint" means that two fail bits are connected in the 8-connectivity and these two fail bits are controlled by one single bit line. The estimated cause step is the bit line contact formation.

Category Mic4:"bit line fail in a sub block" means that fail bits run in a line and its length becomes longer than the specified ratio of sub block width in the direction of bit line. The estimated cause step is the bit line formation.

Category Mic5:"word line fail in a sub block" means that fail bits run in a line and its length becomes longer than the specified ratio of sub block width in the direction of word line. The estimated cause step is the gate formation.

Category Mic6:"bit line fail across two sub blocks" means that fail bits run in a line over the sub block width in the direction of bit line. The estimated cause step is the lower wire (sense amp) formation.

Category Mic7:"word line fail across two sub blocks" means that fail bits run in a line over the sub block width in

the direction of word line. The estimated cause step is the lower wire (driver) formation.

Category Mic8:"block width bit line fail" means that fail bits run in a line and its length is the block width in the direction of bit line. The estimated cause step is the upper wire formation in the bit line direction.

Category Mic9:"block width word line fail" means that fail bits run in a line and its length is the block width in the direction of word line. The estimated cause step is the upper wire formation in the word line direction.

Category Mic10:"cross fail" means that the block width bit line fail cross the block width word line fail. The estimated cause step is the upper wire formation because of the short between upper wires.

Category Mic11:"others" means the failure bit patterns that are not included in the above-described micro level fail patterns.

3.2 Processing

The micro level FBMs are processed by using the proposed pattern recognition method for reducing RAM fail bit map into physical defect data suitable for statistical analysis [1]. The procedure is as follows. Each horizontal line of the map is scanned to failing points. If there are adjacent points, they are combined to form a fail segment. Thus the fail segment list is constructed from the one-pass scan of the map. Each entry in the fail segment list represents a fail segment containing a line number of the segment occurrence and the segment endpoints. After the one-pass scan is finished, these 1-dimensitonal feature components are combined into 2-dimensional feature descriptions by scanning the fail segment list and looking for segments that are adjacent to each other line-to-line; a region list is obtained. Lastly, each entry in the region list is classified into one of 11 categories by their dimensions. The micro level classification list that shows the distribution of fail bit patterns is obtained as shown in Table 2.

4 MACRO LEBEL FAIL PATTERN CLASSIFICATION

In the macro level fail pattern classification, failure patterns are searched in a wafer size data where the fail bit map data is compressed by using a black pixel that represents at least a failed memory bit cell included in the area of 256 bits x 128 bits in the micro level. Macro level fail patterns to be processed are treated in this study as shown in Table 1

4.1 Macro level fail bit patterns

We classify macro level fail bit patterns into 5 categories by considering the characteristics of the manufacturing equipment and their handling of the wafers. Each pattern is defined as follows.

Category Mac1: "inside of single die on outer region" means the failure pattern inside of single die on the outer wafer region. This pattern may be caused by the variation in thickness in the layer formation process, the wafer handling and so on (failure phenomena A).

Category Mac2: "inside of single die on central region" means the failure pattern inside of single die on the central wafer region. It is difficult to specify causes of this failure pattern, since this pattern may occur on any location of the wafer (failure phenomena B).

Category Mac3: "across multiple dies on outer region" means the failure pattern across multiple dies on the outer wafer region. This pattern may be caused by the variation in exposure, the miss shot of stepper and so on (failure phenomena C).

Category Mac4: "across multiple dies on central region" means the failure pattern across multiple dies on the central wafer region. This pattern may be caused by the wafer handling and so on (failure phenomena D).

Category Mac5: "scratch" means the failure pattern like a haze as shown in Fig. 3 (patterns A and B). This pattern may occur when the flow of a fluid on wafer such as the air flows in the diffusion oven becomes nonuniform (failure phenomena E).

4.2 Processing

In order to classify the black pixels in the macro level FBM into 11 categories, we carry out the following image processing.

At first, the objects (black pixels) of the binary FBM image (Image X) are thickened by several pixel widths to connect pixels neighboring each other. The obtained image is referred as Image Y. Next, The objects in the Image Y is labeled. The same labels are given on the corresponding objects on the Image X. Then the objects with the same label on the Image X are gathered into a cluster. On each cluster, a fail density (number of black pixels divided by the area of cluster region) is calculated. Thus the fail cluster list is constructed. Each entry in this list represents a cluster containing a dimensions and a fail density as attributes.

Mac5 pattern is extracted from obtained clusters as follows. At first, clusters with a low fail density are selected. To each selected cluster, the major axis, the major axis angle, the major axis length and the minor axis width are calculated. The clusters with the low ratio of the minor axis width to the major axis length proceed to the next processing. Clusters that have the near major axis angle and the near locations are combined into a Mac5 pattern, that is, "scratch".

After the recognition of Mac5 pattern, other clusters are classified into the rest four categories according to their attributes. Macro level classification result is displayed on a CRT as shown in Fig. 3. Fail bit patterns in each category are shown by using a different color: Mac1 orange, Mac2 green, Mac3 blue, Mac4 yellow, and Mac5 red.

5 CAUSE ESTIMATION

The causes of failure bits are estimated on the comparison of two level classified results with the expert knowledge by the cause estimation system. The procedure is as follows.

At first, an object cluster (fail bit pattern) is selected on CRT that displays the macro level classification result. Then the cause estimation system checks to which category the objective cluster (fail bit pattern) belongs in the macro level classification. Next, fail bit patterns in the objective cluster are classified in the micro level. The micro level classification list is obtained. In this list, the category that has the maximum number of votes is selected. The cause of failures is estimated from Table 1 that is constructed from the expert knowledge. Thus we know that which process in memory production and what phenomenon lead to this fail bit cluster with a high probability.

6 APPLICATION

We applied the system to the FBM of 64M DRAM as shown in Fig. 3. The result of the macro level fail pattern classification showed that parts A and B were classified into a MAC5 category "scratch". Then the part A was analyzed in the micro level classification as shown in Table 2. From the table, it is seen that the "scratch" fail pattern A mainly consists of single bit failures. Thus it is concluded from Table 1 that problematic wafer processing step was channel stopper formation, gate formation, or capacitor formation step where the failure phenomena E was arisen. The times required for the macro level classification of the whole wafer and the macro level classification of part A was 9.36 sec and 10.3 sec on SUN Ultra5 (270MHz), respectively.

7 CONCLUSIONS

We have proposed a fail pattern classification and analysis system of memory fail bit maps in order to determine problematic wafer processing steps rapidly during memory production. The computer directly linked with the memory tester is not used. The system mainly consists of three procedures, the macro level failure pattern classification, the micro level failure pattern classification and the cause estimation based on the comparison of two level classified results with the expert knowledge. In the micro level, the failure patterns are classified into eleven categories. In the macro level, the failure patterns are classified into five categories by utilizing image processing algorithm such as thickening, labeling, and clustering. The system was applied to fail bit map data from recent DRAM devices to show its validity.

REFERENCES

[1] M. Faucher, "Pattern recognition of bit fail maps," Proc. International Test Conference, pp.460-463, 1983.

[2] S.P. Cunningham and S. MacKinnon, "Statistical methods for visual defect metrology," IEEE Transaction on Semiconductor Manufacturing, **11**, 1, pp.48-53, 1998.

[3] T. Tsujide, et al., "Automatic memory analysis using an expert system with a memory tester/analyzer," Proc. International Test Conference, pp. 184-189, 1993.

[4] M. Sugimoto, H. Hamada, and T. Hamada, "High-speed processing system for memory failure analysis," NEC Technical Journal, **50**, 6, pp.11-15, 1997.

Figure 3: Example of 64M DRAM FBM.

Table 2: Result of the micro level classification of part A in Fig. 3.

Micro level fail pattern items	
Single bit fail	174
8-connected two bits fail with an address constraint	0
8-connected two bits fail with no address constraint Cross fail	1
Bit line fail in a sub block	0
Word line fail in a sub block	0
Bit line fail across two sub blocks	0
Word line fail across two sub blocks	0
Block width bit line fail	0
Block width word line fail	0
Cross fail	0
Other bit line fail	0
Other word line fail	0
Others	4