Investigation of the Mechanism of Floating Node Assisted CMOS Latch-Up

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ABSTRACT

A new phenomenon of floating node assisted CMOS latch-up is experimentally observed and investigated using TCAD simulation.

Using test structures having parasitic bipolar transistors and an electrically floating N+ diffusion node located at various distances from a power supply node, we observed clear snapback to a low impedance state when the floating node approaches within a few microns of the power supply node.

Through TCAD simulation, we found that this floating node behaves like a virtual cathode of a PNPN structure when high enough field is sustained by the underlying high resistance well. Under this high field, the diffusion node is no longer electrically floating but virtually connected to the neighboring power node by avalanche breakdown.

We conclude that floating diffusion nodes can enable latch-up, if located within a few microns of a power supply node.

Keywords: latch-up, floating node, TCAD, SCR, ESD

1. INTRODUCTION

Because of the widespread adoption of the chemical mechanical polishing (CMP) process for sub-micron VLSI manufacture, there has been an increasing requirement for dummy metal or dummy diffusion patterns to improve global planarization [1]. Moreover commercialization of sophisticated optical proximity correction (OPC) software tools make it practical to compensate local variation of critical dimensions, by balancing the pattern density with dummy patterns.

But the effects of the dummy patterns, especially when they are electrically floating, on the reliability of nearby circuits and propagation delay or cross talk of signal lines are not fully understood. The dummy patterns are electrically floating in order to optimize design time and cost [2]. However, one of the undesirable side effects of such floating dummy diffusion patterns can be to make latch-up more likely during transient power fluctuations.

In this study we determined experimentally the effect of a floating N+ diffusion node located at various distances from a power supply node on the latch-up behavior. Using TCAD simulation, we investigated the mechanism of the enhanced latch-up.

2. EXPERIMENT

The test structure described in Figure 1 was fabricated using a conventional 0.8 μm 30-volt CMOS P-well technology. A floating N+ diffusion of size 5 μm x 60 μm is placed 9 μm away from an N-base diffusion. The space between the floating N+ and the P+ diffusion connected to the V_{SS} power supply was varied from 0 μm to 4 μm. The V_{cc} node has both P+ and N+ diffusions. This P+ connected to V_{cc} is the emitter of a parasitic vertical PNP. In this configuration the vertical PNP and the lateral NPN, which are the inevitable parasitic bipolar transistors

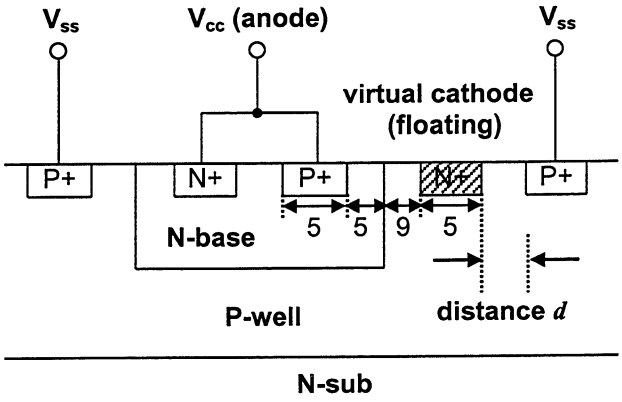

Figure 1: Cross sectional description of test structure. In the conventional well structure, electrically floating N+ diffusion node is inserted. The distance from the node to V_{ss} power node is varied. Numbers indicate horizontal dimension in units of μm.

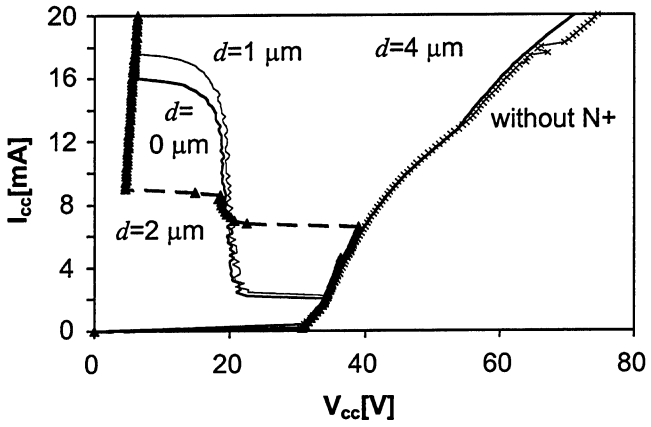

Figure 2: Measured I-V characteristics of the test structure show dependence on the distance between floating node and nearby V_{ss} node.

formed in CMOS technology, forms the usual PNPN semiconductor-controlled rectifier (SCR) structure. In the usual SCR the shaded N+ node is connected to V_{ss} instead of floating.

To see the effect of this floating node at the high injection condition of vertical PNP bipolar transistor, we measured I-V characteristics of this test structure. Results shown in Figure 2 indicate that as the N+ diffusion node approaches the V_{ss} power node, there is clear snapback phenomenon even though there is no apparent cathode for the latch-up mechanism. When the distance from N+ to V_{ss} is greater than 2μm or there is no N+ node, latch-up does not occur. By this experiment, we confirmed that a floating diffusion node could participate in the latch-up of a CMOS device, if it is located closely enough to the power node.

3. TCAD SIMULATION

To investigate the detailed mechanism of this snapback, we used TCAD simulation. First by comparing the measured and simulated I-V characteristics of standard PNPN structure in which N+ diffusion node is connected to V_{ss} node, we confirmed our TCAD input file in terms of process condition and simulation methodology. Figure 3 shows the result of this simulation. Triggering voltage and holding voltage match with measured data for this PNPN SCR structure. At the triggering condition (middle of Figure 3), N-base to P-well breakdown dominates the current of this device, but at the holding condition (bottom of Figure 3) PNP and NPN parasitic bipolar emitters, which are forward biased by potential drop through well resistance, dominate the current from V_{cc} to V_{ss}.

Based on this input file, we did various TCAD simulations for the floating node case.

In this simulation we found that P-well depth and doping also play key role in the latch-up of this structure. When there is no floating N+ diffusion node, or when the P-well is deeper or absent (in other words P-substrate which

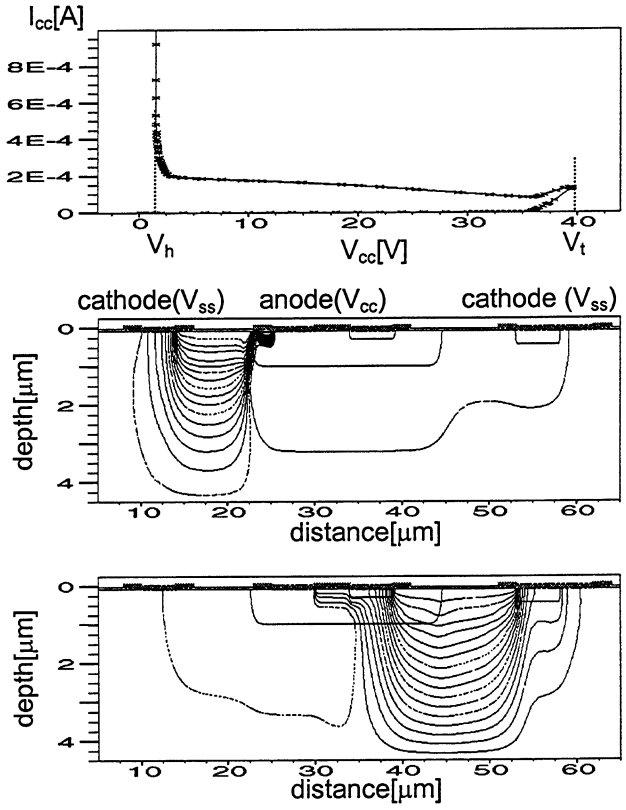

Figure 3: Simulated I-V characteristics (top), cross sectional current flow lines at triggering condition (middle) and holding condition (bottom) of the usual PNPN structure.

is extreme case of deeper P-well) latch-up does not occur. This simulation result agrees with measurements performed on wafers with P-substrate instead of P-well. The TCAD results in Fig.4 show that floating node induced latch-up occurs only when P-well depth is shallow enough.

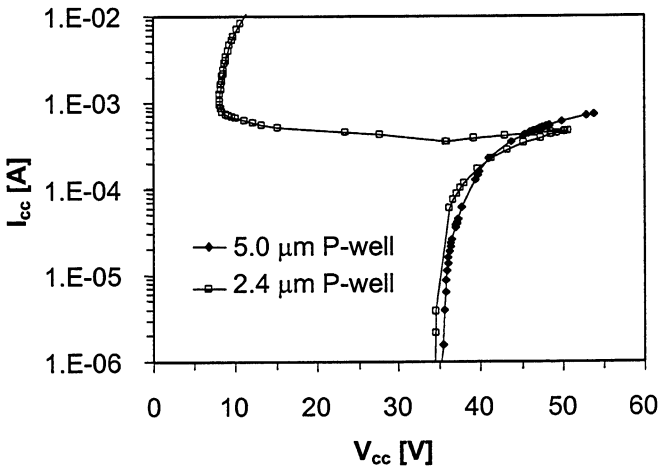

Figure 4: I-V curve generated by TCAD simulation for two different P-well depths with floating N+ nodes. Only in case of 2.4μm P-well, latch-up phenomenon is observed.

For qualitative explanation of this novel phenomenon of floating node assisted latch-up, we constructed schematic diagram as shown in Figure 5. This schematic is similar to a conventional SCR except for an additional diode at the N+ diffusion node [3]. At the triggering voltage, N-base to P-well junction goes into avalanche breakdown condition which is the same as shown in middle of Figure 3. This current builds sufficient potential drop across N-base and P-well resistance so that the emitter of the vertical PNP is forward biased and lots of holes are injected into the P-well. As this hole current flows through the P-well resistance R_p, there is a potential drop of $I_{Rp}R_p$ between base of Q_{npn} and V_{ss} node. Since the potential of floating N+ node cannot be more than one diode drop (V_f) lower than that of base of Q_{npn}, there is a potential drop of $I_{Rp}R_p$–V_f between N+ floating node and V_{ss} node. This amount of voltage reverse-biases diode D_1. So in this high voltage triggering condition, this diode goes easily to avalanche breakdown status driving Q_{npn} into its active region. So both Q_{pnp} and Q_{npn} become forward biased and makes low impedance state, if

$$\beta_{npn}\beta_{pnp} > 1 + \frac{(\beta_{npn}+1)(I_{Rp}+I_{Rn}\beta_{pnp})}{(I_{CC}-I_{Rp})}$$

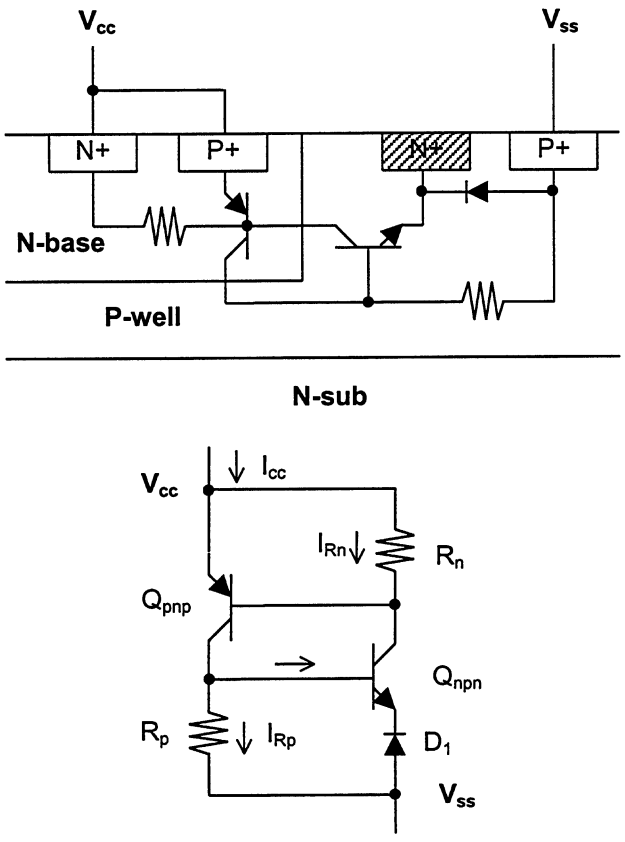

Figure 5: Schematic circuit diagram drawn on cross sectional view can be considered as an SCR structure with a diode addition at the emitter side of NPN transistor.

condition is met, where β_{npn} and β_{pnp} are the common emitter current gains of parasitic NPN and PNP transistors [4]. I_{Rp} and I_{Rn} are currents flowing through P-well and N-base resistance respectively, which are approximately $(V_f + V_{BV})/R_p$ and $(V_f)/R_n$.

To verify this hypothesis, we investigated electric field and impact ionization rate in this device at the latch-up condition. As shown in Figure 6 there is an extremely high field (~1MV/cm) near the surface of the N+ floating node, which is enough to cause avalanche junction breakdown. Current flow lines shown in Figure 7, also support this hypothesis. The role of N+ floating node is to provide sufficient electrons to the P-well by avalanche breakdown, which is sustained by high electric field at holding condition. Since the holding voltage is pretty high (5 ~ 10V), it can cause permanent damage on devices or malfunction of circuits in high voltage devices. On the other hand this structure can be used as an ESD protection device, and the holding voltage can be controlled above the breakdown voltage of N+ junction so that there is no possibility of evolving into hazardous latch-up after the ESD shock has gone. We conclude that floating diffusion nodes can enable latch-up, if located within a few microns of a power supply node.

4. CONCLUSION

We have demonstrated that in a P-well process, a floating N+ diffusion can enable latch-up if it is located within a few microns of a power supply diffusion.

The conditions necessary for latch-up were found by building test structures with various N+ to P+ spacing.

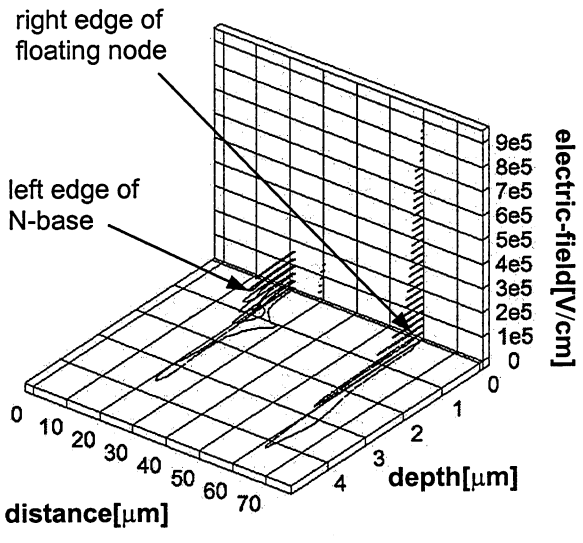

Figure 6: 3-D plot of electric field at holding condition showing extremely high field around right side of N+ floating node.

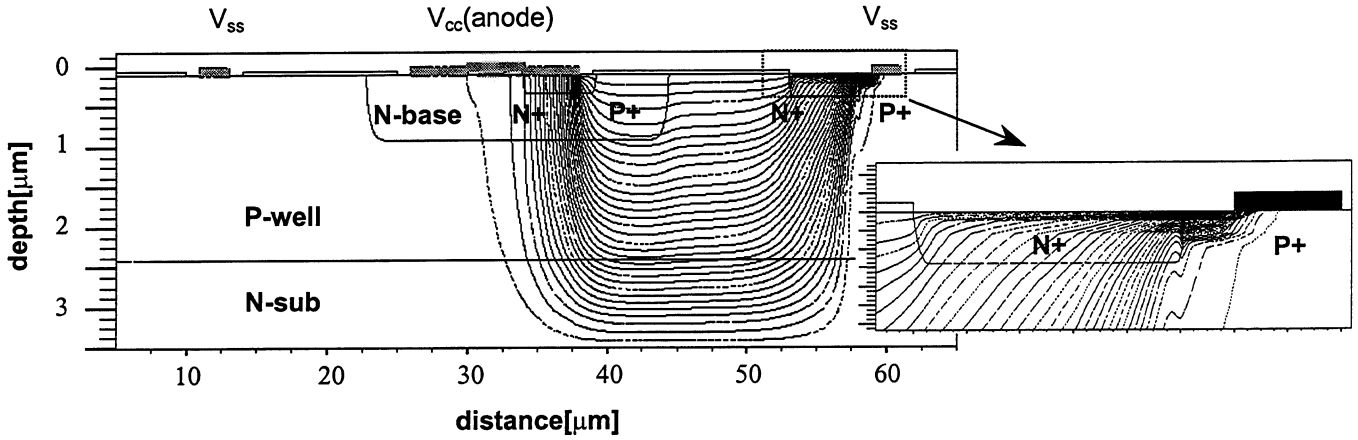

Figure 7: Current flow lines at holding condition of the PNPN structure with a floating N+ diffusion node. Current flows out from V_{cc} node, going through N+ floating node left to right and arrives at V_{ss} node. The magnified view of dotted box shows clearly the current flow through floating N+ diffusion node.

When the distance was 2 μm or less, latch-up was observed. We also found that the P-well depth is an important factor. When the P-well is 5 μm deep or deeper, latch-up did not occur.

The mechanism of this floating node assisted latch-up was investigated and explained by using TCAD simulations. In the latched state, the floating N+ is no longer electrically floating but virtually connected to the neighboring power node by avalanche breakdown. The operation is somewhat similar to a conventional SCR.

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