A Method for Determining the Dependence of Integrated Circuit Performance on Silicon Process, Device and Circuit Parameters

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ABSTRACT

The goal of this project is to develop a structured methodology for achieving a design of a block of circuit in an IC which is more compliant to the specification using a multiple simulation approach. This has been accomplished by developing a statistical design and simulation methodology. This methodology has been demonstrated by simulating a Bipolar Low Noise Amplifier (LNA) circuit using micro-level semiconductor device parameters and associated manufacturing process parameters for the circuit parameters of interest. The physics-based device and process models are then coupled with proprietary statistical simulation software (STADIUM©) to create a robust circuit design which gives rise to a more compliant product with higher yields.

Keywords: Modeling, Simulation, Statistical Design, Wireless Communications, Semiconductor IC Manufacturing.

1 INTRODUCTION

Given the complicated and intricate nature of ICs, the work presented in this paper brings together for the first time a variety of research ideas from many different interdisciplinary areas including semiconductor device engineering, applied statistics and circuit design. Semiconductor chip companies, engineering research organizations, and academic institutions have been heavily investigating the methods to reduce IC product development cost and cycle time [1-5]. There are several widely used circuit simulation software packages, such as *SPICE* or *SPECTRE,* used by circuit designers, as well as, silicon-processing simulation packages, such as *SUPREM,* used by silicon process engineers. These tools help designers to some level of prediction of silicon processing results and semiconductor chip performance on a particular technology. Because of the unknowns in the analysis, there are usually costly design changes and schedule delays, which one would like to reduce and avoid.

2 METHODOLOGY

The project undertaken has developed a new methodology to achieve enhanced circuit designs using a design of experiments multiple simulation approach. The goal of this project is to develop a structured methodology, as shown in Fig.1, for achieving the design of a circuit, which is more compliant to the specifications of the product. One of the most important objectives of this study was creating micro-level semiconductor device models via MATLAB™ that are incorporated into electrical circuit simulation. These physics-based device and process models are then coupled with unique statistical simulation software called STADIUM [6-10] to create a robust circuit design which gives rise to a more compliant product with higher yields. STADIUM , a software program which couples computer simulators to a highly strong statistical method so called design of experiments or DoE. This software uses DoE to estimate statistical variability information from a simulation system which would normally not generate statistical results. The most crucial aspect of the STADIUM is its ability to identify the important variables and how important they are to the problem being analyzed. It simplifies the task of a researcher who is unfamiliar with the DoE. STADIUM allows the engineer to employ a number of different design of experiments options in a very easy to use format. It can be utilized in a number of applications and simulation environments, which exist in industry and basic research conducted by government and academics. As a result of this tool and new methodology developed in this work, the gap among circuit designers, wafer process engineers, and semiconductor device modeling engineers will be narrowed.

3. DEMONSTRATION OF THE METHODOLOGY

The choice of circuits to demonstrate this new statistical approach is a 2.4 GHz bipolar low noise amplifier as shown in figure 2. This prototype single stage , common emitter, class A, npn high frequency low noise amplifier was built on a 0.6 μm BiCMOS Ultra High Frequency (UHF) technology for low cost mixed-signal RF applications with an f_t of 25 GHz and was described in detail elsewhere [11].

This LNA contains input matching components of a capacitor of C_1 and an inductor of L_1, output matching components of C_2 and L_2, a npn bipolar transistor Q_1, and a current source of I_1. The capacitor C_1 is DC blocking capacitor while C_2, L_1 and L_2 are utilized for on-chip matching for the input and output, respectively [12]. The Q1 transistor is the RF common emitter amplifier located in the signal path and is optimized to run at a desired collector current by individual components of the I_1 current source

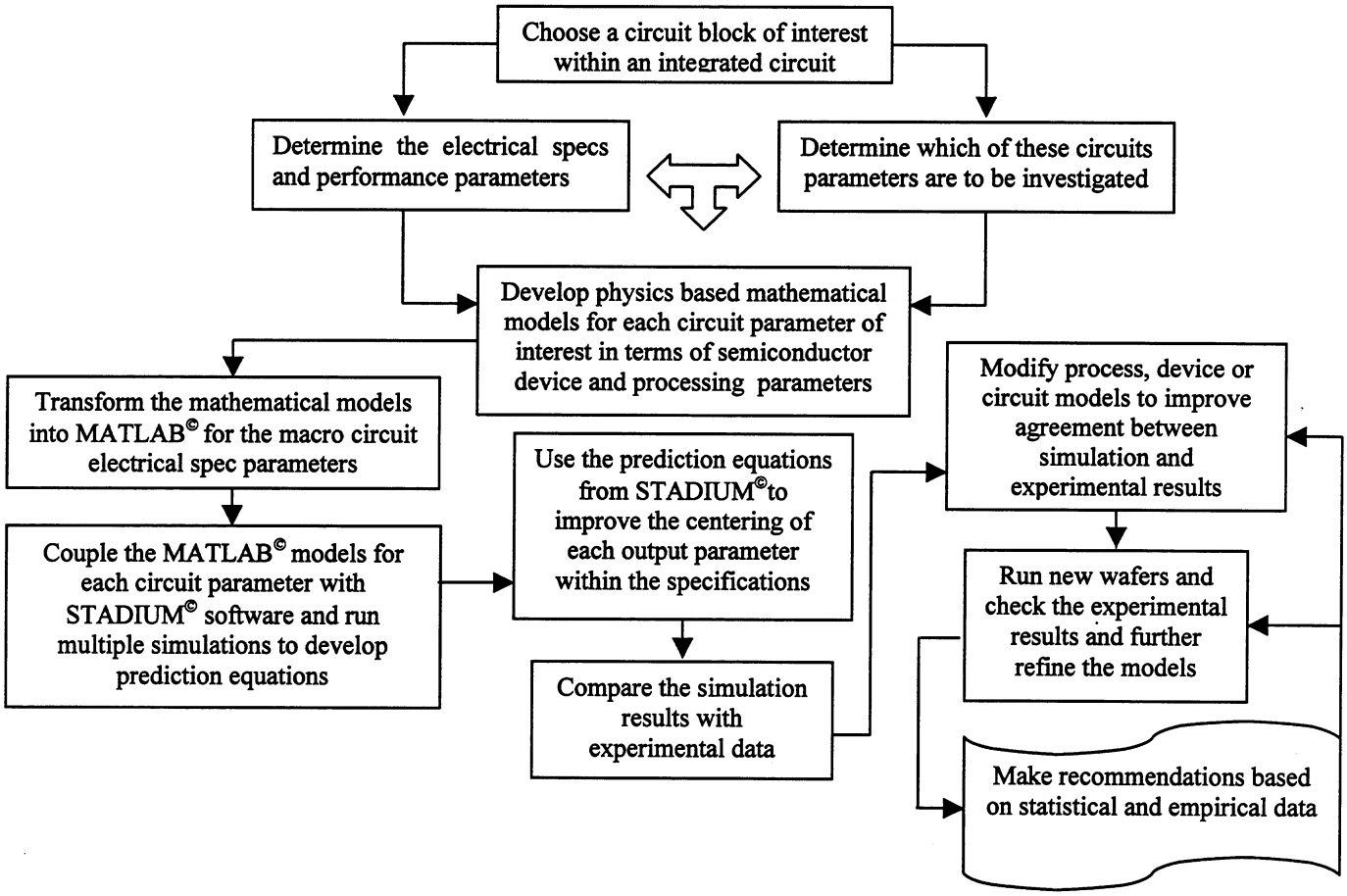

Figure 1: The flow diagram for the "*top to bottom*" approach.

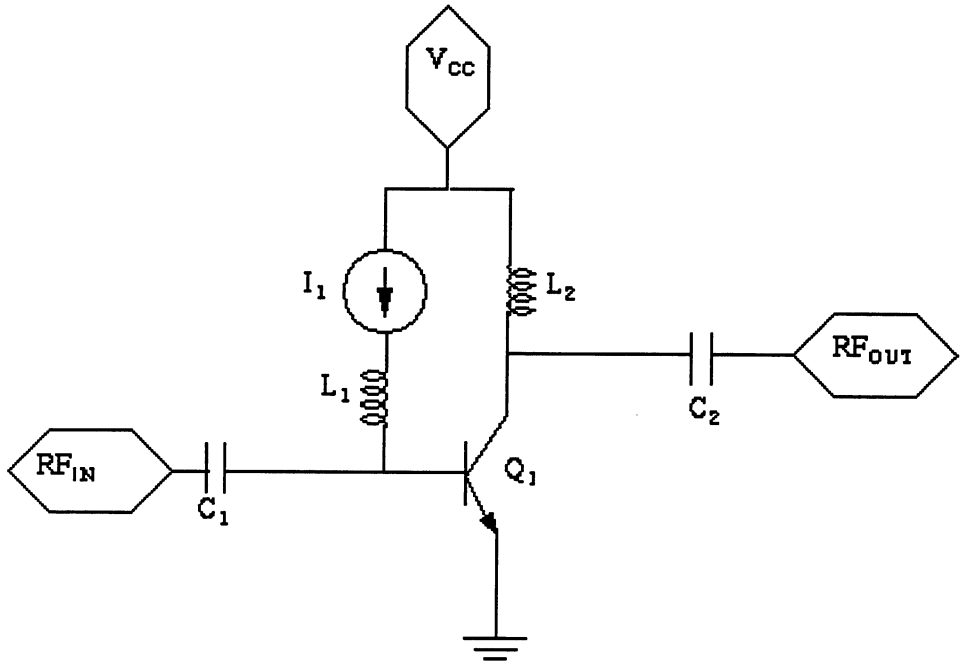

Figure 2: A simplified circuit schematic of the Low Noise Amplifier under study

which will not be reported here. These LNAs have been recently and widely used in many applications [13-15]. These application areas include 1.8-1.9 GHz wireless personal communication systems. These low noise amplifier circuits were characterized in terms of electrical circuit parameters such as noise figure (NF), power/voltage output gain, and output gain compression or the third order intercept point. These are shown in Table 1.

Symbol	Parameters	Min	Typ	Max	Sim
Av (dB)	Output gain	17	20	23	22.2
NF (dB)	Noise Figure		2	3	5
IP3o (dB_m)	The third order intercept point	12			15.6
f (GHz)	RF frequency	2.4	2.45	2.5	2.45
V_{cc} (V)	Supply Voltage	2.7	3.0	3.3	2.7

Table 1: Three final output electrical parameters over operation frequency and supply voltage. The last column shows circuit simulation data.

The next step was to obtain the circuit equations for these parameters. As the circuit designer described [12], the output gain A_v , one of the LNA specs, can be given by the following expression,

$$A_v=20\log\{\sqrt{\frac{Vp\beta^3Vt^3C\pi Icc^2+Vp\beta^2Vt^2Icc^3}{(IccVt\beta+\beta Icc^2Ze+IccZe\beta VtC\pi+Icc^2Ze)(2Vt^2\beta C\pi+2VtIcc)^2}}\}$$

In this work, physics based mathematical models for the each circuit spec output parameter characterized and represented by semiconductor device and processing parameters, such as

$$\beta=\frac{\alpha}{1-\alpha}=\frac{\gamma\beta_T}{1-\gamma\beta_T}$$

$$\beta_T=1-\frac{1}{L_n^2}\int_0^{x_B}(\frac{1}{N_a}\int_x^{x_B}N_a dx)dx$$

$$L_n=\sqrt{D_n\tau_n}$$

$$D_{n,p}=\frac{kT}{q}\mu_{n,p}$$

$$\gamma=(1+\frac{D_pN_ax_B}{D_nN_{dE}x_{jE}})^{-1}$$

$$x_B=x_{jB}-x_{jE}$$

$$x_{jB}^2=4Dt\ln\frac{Q_B}{N_c\sqrt{\pi Dt}}$$

$$Q_B=\int_0^{x_{jB}}N(x)dx$$

$$\rho_s=\frac{\rho}{x_{jB}}=\frac{1}{q\mu_{eff}\int_0^{x_{jB}}N(x)dx}\approx\frac{1}{q\mu_pQ_B}$$

$$V_p=\sqrt{2}(V_{cc}-V_{ce}) \qquad V_t=kT/q$$

$$C_\pi=(C_{je}W_e+\tau_f g_m)$$

where

$$C_{je}=A[\frac{qK_s\varepsilon_0N_d}{2(V_R+\psi_0)}]^{1/2}\approx\frac{K_s\varepsilon_0A}{x_d}$$

$$\tau_f=x_B^2/2D_n$$

$$g_m=I_{cc}/V_t\approx[I_s exp(V_{BE}/V_t)]/V_t$$

$$Z_e=r_e/W_e+L_e\omega j$$

Symbol	Input Parameter	Low	High
N_a (cm^{-3})	Doping concentration in Base	6E17	6.2E17
N_{dE}(cm^{-3})	Doping concentration in Emitter	3E18	3.2E18
V_{ce} (V)	CE voltage	0.9	1.0
I_{cc} (A)	DC operating supply current	15.0	15.2
W_e (μm)	Emitter width	30	35
r_e (Ω.m)	Emitter resistance	25E-6	30E-6
L_e (H)	Emitter and lead inductance	1E-9	1.1E-9
V_{cc} (V)	Supply voltage	2.7 or 3.0 or 3.3	
f (GHz)	Operation frequency	2.4 or 2.45 or 2.5	
Q_B	Bulk charge	const.	
T	Diffusion time	const.	
T_d	Diffusion temperature	const.	
D	Diffusion coefficient	const.	
N_c	Doping concentration in Collector	const.	
D_n & D_p	Diffusion constant for electrons & holes	empirically calculated	
τ_n	Life time of electrons	2.5E-3	
τ_p	Life time of holes	2.5E-3	
x_{jB}		0.433E-4	
x_{jE}	Emitter junction depth	0.316E-4	
C_{je}	Emitter-Base junction depletion cap	2.9E-9	
r_b	Transistor noise base resistance	616E-6(Ω.m)/We	
T	Operation temperature	25 °C	

Table 2: Overview of input parameters and their randomly selected low and high values for STADIUM statistical simulations.

Similarly, the output compression point, OpdBm, is an intermediary output parameter,

$$OpdBm=10\log\{\frac{Vp'Icc^2}{2(\beta Vt|C\pi|+Icc)10^{-3}}\}$$

$$P1dB=OpdBm-1$$

or the third order intercept point IP3o, as an output parameter

$$IP3o=P1dB+10.$$

The third spec, Noise Figure (NF) has been defined as follows,

$$NF=10\log\{\frac{2\beta^2 I_{cc}V_t(|Z_y|)^2(R_{in}+r_b+RE)+(|Z_y|)^2(|Z_x|)^2+4R_{in}^2\beta I_{cc}^2(|Z_x|)^2}{2R_{in}\beta^2 V_t I_{cc}(|Z_y|)^2}\}$$

$$Z_y=2R_{in}\beta V_t C_\pi+2R_{in}I_{cc}+\beta V_t$$

$$Z_x=2R_{in}\beta V_t C_\pi+2R_{in}I_{cc}-\beta I_{cc}Z_e$$

Symbol	Intermediary Output Parameters
V_p	Output voltage
β	The common emitter current gain
C_π	Base Emitter capacitance
R_{in}	Input impedance
$OpdB_m$	Output compression point

Table 3: List of simulated intermediary output parameters.

Then, these models have been transformed into *MATLAB* to generate macro circuit electrical spec models for an input to couple with the statistical simulation software *STADIUM.* The input and intermediary output parameters are shown in Tables 2 and 3, respectively. The first seven input parameters listed in Table 2 have been assigned variations. Then these seven input variables have been used to run multiple simulations using a statistical designed experiment of fractional factorial resolution 3 over operation frequency and supply voltage. The factor contributions of these variables for each three output parameters along with mean and standard deviations have been calculated and compared to measurement values. These are summarized in Table 4.

Parameter	Calc. Mean this work	σ	Meas	Meas σ	Circuit Sim
Av (dB)	21.84	0.31	16.44	0.19	22.2
NF (dB)	3.79	0.07	4.4	0.15	5
IP3o (dB_m)	15.03	0.21	16.21	0.26	15.6

Table 4: Comparison of mean and standard deviation values of actual measurements and circuit simulation results performed at 2.7 V at 2.45 GHz versus the calculated values obtained via statistical simulations in this work.

CONCLUSIONS

One can clearly observe the excellent agreement between calculated at this work versus circuit simulation value of output gain which is within spec. The noise figure and the third order intercept point are very good correlated with circuit simulation and measurement values. Selecting new set of low and high values for these influential input parameters will increase the sensitivity of statistical design of the low noise amplifier for desired specifications. Thus, results of this analysis give the statistical dependence of these output parameters on the semiconductor device and silicon processing parameters and leads to optimum solutions for the LNA circuit design and manufacturing flow.

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