A model for fully depleted double gate SOI MOS transistors including temperature effects

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Abstract

A model for a fully depleted double gate Silicon on Insulator (SOI) Metal Oxide Semiconductor (MOS) Transistors is presented. Small geometry effects such carrier velocity saturation, mobility degradation, and channel length modulation are included. Both lattice and carrier thermal effects are considered. The effect of temperature is included in device mobility, threshold voltage, and intrinsic carrier concentration. The modeled results are studied to isolate the importance of lattice and carrier temperature on device characteristics. It is noticed that lattice temperature effects play a much greater role for devices up to 100 nm. The effects of carrier temperature would be significant and may not be ignored for device sizes below 100 nm. Saturation region is modeled including the effects of impact ionization current and parasitic bipolar transistor. Unlike earlier models the present model insures the continuity of drain current and drain conductance at the point of transition from the linear to saturation region.

1. Introduction

Fully depleted SOI MOSFETs have advantages of ideal subthreshold slope, reduced channel and body effects, increased transconductance, higher speeds, higher packaging density, built in device isolation, and latch up free. Disadvantages are parasitic bipolar effect due to floating body effects and self heating due to lower thermal conductivity of buried oxide layer can be of serious concern for IC application.

Double gate SOI MOSFETs in which channel is controlled by front and back gate, as shown in fig. 1., has the potential of smaller geometry compared to single gate MOSFETs [1]. In this work a model for fully depleted double gate SOI MOSFET is presented. Important small geometry effects such as carrier velocity saturation, channel length modulation, mobility degradation, drain induced barrier lowering, and series resistances are accounted for. Parasitic bipolar effects and hot carrier effects are also included in modeling drain current in the saturation region.

In SOI MOSFETs low thermal conductivity of buried oxide layer give rise to self heating problem. Major device parameter such as carrier mobility, threshold voltage, and intrinsic carrier concentration are temperature dependent. In this study thermal effects are included in mobility, threshold voltage and intrinsic carrier concentration expressions.

Saturation parameters such as Esat, VDsat are found by insuring continuity of drain current and drain conductance at the point of transition from linear to saturation regime. The accuracy of developed model is verified by comparing modeled results to available experimental data in literature.

2. Device Characteristics

Quasi-two dimensional approach is adopted. The device under consideration, as shown in Fig. 1, is partitioned into two regions. In Region (I) gradual channel approximation is applied. The region (II) is extended from the point of saturation (l_{eff} - ΔL) to the drain (l_{eff}).

2.1 Thermal Effects

In SOI MOSFETs the low thermal conductivity of buried oxide layer gives rise to self-heating effects. This effect may cause serious problems in VLSI applications. In this part of the study charge carriers and lattice are considered at thermal equilibrium ($T_l = T_n$). The carrier mobility as function of lattice temperature is given by [2].

$$\mu_n = \frac{\mu_s(T_l)}{1+\alpha\frac{k}{q}(T_n - T_l)}\Big|_{T_n=T_l} = \mu_s(T_l) \qquad (1)$$

Where

$$\mu_s(T_l) = \mu_{s0}\left(\frac{T_l}{T_0}\right)^{-2}$$

μ_{s0} is the carrier surface mobility at room temperature. Carrier velocity saturation which is a major small geometry effect and excluded in earlier modeling of SOI MOSFETs[3,4] has been accounted for in this study. The mobility equation in the linear region which accounts for carrier velocity saturation is approximated by:

$$\mu_{s0}=\frac{\mu_0}{1+\theta(V_G-V_T)}\frac{1}{1+\frac{E_y}{E_c}} \quad (2)$$

μ_0 is the low field mobility, θ is the mobility reduction factor due to the vertical field, E_c is the critical field, and V_T is the threshold voltage.

The lattice temperature related to power dissipation in the device given by [5].

$$PR_{th}=T_l-T_0 \quad (3)$$

Simple algebraic manipulation would lead to:

$$\mu_s(T_l)=\mu_{s0}[1+\frac{PR_{th}}{T_0}]^{-2} \quad (4)$$

where thermal resistance is given by [5]

$$R_{th}=\frac{1}{2W}(\frac{t_{box}}{K_{ox}K_d t_{si}})^{\frac{1}{2}} \quad (5)$$

Where P=I.V, t_{box} is the thickness of buried oxide, K_{ox} is the thermal conductivity of oxide, K_d is the thermal conductivity of silicon, t_{si} is thin silicon layer, and W is the channel width.

2.2 I-V Characteristics in the Linear Region:

The drain current in the linear region is found by integrating the product of the carrier velocity and mobile channel charge over the effective channel length.

$$I_{DL}=2\frac{W\mu^*C_{ox}}{L_{eff}+\frac{V_{DS}}{E_c}}[(V_G-V_T)-a_0V_{DS}]V_{DS} \quad (6)$$

$$a_0=\frac{1}{2}[1+\frac{\epsilon_{si}}{\epsilon_{ox}}\frac{t_{ox}}{t_{si}}]$$

Threshold voltage which takes into accounts the drain induced barrier lowering is given by [6]:

$$V_T(T_l)=V_T(T_0)-\Delta V_T$$
$$\Delta V_T=K_4(T_l-T_0) \quad 0.5mVK^{-1}<K_4<4mVK^{-1} \quad (7)$$

2.2.1 Effect of Series Resistances

Effects of the drain, the source, and the channel series resistances are included by following modifications to appropriate terminal voltages.

$$\hat{V}_{GS}=V_{GS}-I_{DS}R_s \;;\; \hat{V}_{DS}=V_{DS}-I_{DS}R_T$$
$$R_T=R_S+R_D+R_{ch} \;;\; R_{ch}=\frac{V_{DS}}{I_{DS}} \quad (8)$$

Substituting expressions of eq. (8) into eq. (6) and performing few algebraic manipulations would result in:

$$I_{DL}=\frac{4X_3}{X_2+(X_2^2-4X_1X_3)^{\frac{1}{2}}} \quad (9)$$

where

$$X_1=R_SR_T+\frac{\beta}{E_c}R_T-a_0R_T^2$$
$$X_2=(V_G-V_T)R_T+V_{DS}(R_S+\frac{\beta}{E_c}-2a_0R_T) \quad (10)$$
$$X_3=(V_G-V_T)V_{DS}-a_0V_{DS}^2 \;;\; \beta=\frac{1}{2W\mu^*C_{ox}}$$

2.3 Saturation Region

The drain current in the saturation region consists of three different components.

$$I_T=I_{DSS}+I_{Bip}+I_{imp} \tag{11}$$

I_{DSS} is the drain current in the saturation region in the absence of both parasitic bipolar and impact ionization current effects:

$$I_{DSS}=I_{DSL}\big|_{V_D\to V_{Dsat},\ L\to L-\Delta L} \tag{12}$$

I_{bip} is due to parasitic bipolar effects and is given by [7].

$$I_{Bip}=\alpha I_E+I_{CBO} \tag{13}$$

$$I_{CBO}=Wt_{si}\frac{I_{so}}{1+\theta_f(V_G-V_T)} \tag{14}$$

The leakage current is given by [5].
I_{imp} is the impact ionization current and is given by [8].

$$I_{imp}=\int_{L_{eff}-\Delta L}^{L_{eff}} I_D\alpha_0\exp(-\frac{\Delta}{E_y})dy \tag{15}$$

The channel length modulation, ΔL, is found by applying Gauss's Law to the two-dimensional drain region (Region II of Fig. 1).

$$-\int_0^{X_1}\epsilon_s E_{sat}dx+\int_0^{t_{si}}\epsilon_s E_y dx-2\int_0^{y}\epsilon_{ox}E_{ox}dy= -q\int_0^{y}[\int_0^{t_{si}}(n+N_A)dx]dy \tag{16}$$

Differentiating above equation and using E_y = - dV/dy, and rearranging terms while using approximation that would not compromise the model accuracy yields:

$$\frac{d^2V}{dy^2}=-\frac{1}{\lambda^2}[V_G-\eta(\frac{V_D+V_{Dsat}}{2})]+\frac{q}{\epsilon_s}(N_A+n);\qquad 0<\eta<1 \tag{17}$$

$$\lambda=\sqrt{\frac{\epsilon_s}{2\epsilon_{ox}}t_{si}t_{ox}}$$

where λ is defined as the natural length [9].
Applying boundary conditions $E_y = E_{sat}$, $V_y = V_{Dsat}$ at y = L-ΔL and $V_y = V_D$ at y = L, results in

$$\Delta L=\sqrt{(\frac{E_{sat}}{\Omega})^2-\frac{2(V_D-V_{Dsat})}{\Omega}}-\frac{E_{sat}}{\Omega} \tag{19}$$

$$\Omega=\Gamma\eta(\frac{V_D+V_{Dsat}}{2})-\xi\ ;\quad \Gamma=\frac{1}{\lambda^2}$$

$$\xi=\Gamma V_G-\frac{1}{\epsilon_s t_{si}}\frac{I_{Dsat}}{W v_{sat}}-\frac{qN_A}{\epsilon_s}$$

The drain voltage at the point of saturation is found by insuring continuity of the drain current and the drain conductance at the point of transition from linear to saturation.

Accuracy of this work is verified by comparing modeled results to measured data [5]. Figures [2] and [3] show drain current and transconductance over wide range of operating voltages. These results show a v. good match between modeled and measured data. It is important to point to negative drain conductance which is due to increase in device temperatures caused by low thermal conductivity of buried oxide layer in SOI MOSFETs.

3. Conclusion

An accurate analytical model, in the strong inversion regime, for small geometry fully depleted SOI MOS transistors at room temperature is presented. Major small geometry effects and series resistances are included. Parasitic bipolar effects, and impact ionization current are

included in modeling drain current in saturation region. Discontinuity in drain conductance is avoided. The accuracy of the model is verified by comparing modeled results to available measured data. Presented model is accurate and yet computationally efficient which makes it a good candidate for use in integrated circuit simulation software. It is noticed that the lattice temperature effects play greater role in modeling devices down to 100nm. It may be necessary to include carrier temperature effects for devices below 100nm to achieve greater model accuracy.

References

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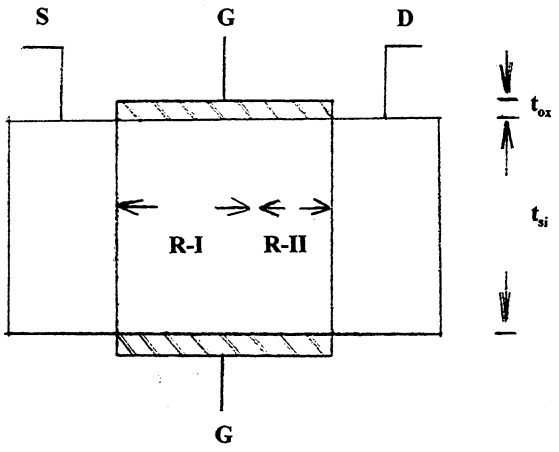

Figure 1. Cross-section of Double Gate SOI MOSFET

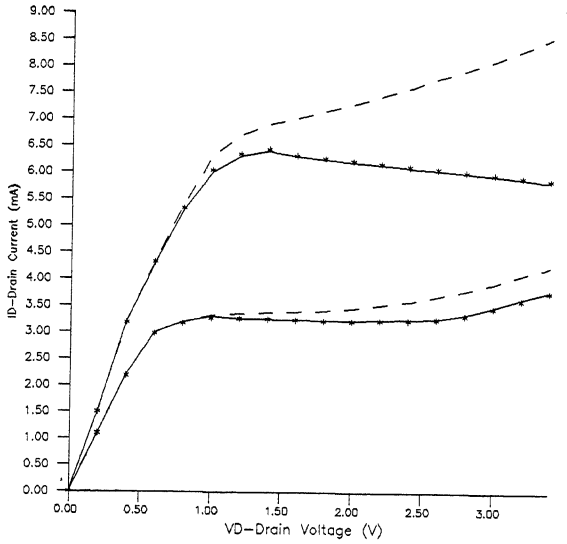

Figure 2.The drain current vs. drain voltage, for V_G= 2.2, 3.3Volts. L=0.33μm, W=10μm. *-exper. Results, solid line is modeled results, dashed line is modeled results without thermal effects.

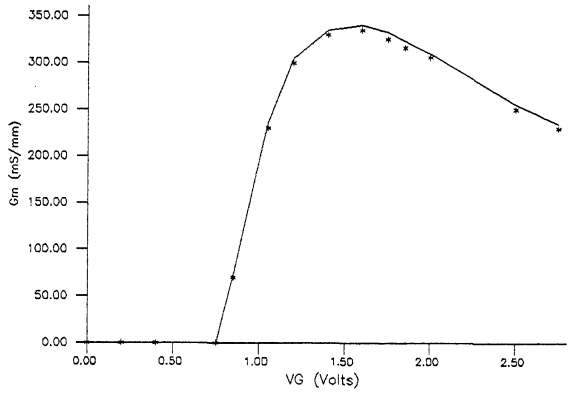

Figure 3. The transconductance vs. Gate voltage for V_D= 2.0 Volts. *- experimental results, solid line is modeled results including thermal effects.