Towards a Compact Scattering Model for Nanoscale MOSFETs

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Abstract: A new compact model for nanoscale MOSFETs based on scattering theory is proposed for the full range of V_{GS} and V_{DS} covering sub-threshold, linear and saturation regions of operation. Quantum confinement and carrier degeneracy are fully accounted for in this model. The model is continuous above and below threshold and from the linear to saturated regions. It works all the way to ballistic limit. Using this model, the *I-V* characteristics of a symmetric Double Gate MOSFET are simulated and compared with 2D numerical simulation. The analytical model shows good agreement with full 2D simulation.

I. INTRODUCTION

MOSFET technologies now under development have channel lengths well below 100nm where near-ballistic operation becomes feasible [1]. But device development and circuit simulation continue to be based on traditional MOS models whose physical basis is losing validity as channel lengths shrink below 100nm. In this paper we develop a new kind of compact model for the MOSFET – one that has a strong physical basis that should continue to be valid as MOSFET dimensions shrink to their limits.

In this paper, we extend our previous work, which introduced an elementary scattering model for the saturated current [2] and separately for the linear-region current [3]. These models were useful conceptually but incomplete because they did not cover the full *I-V* characteristic, and they were expressed in terms of a backscattering parameter, *r*, whose functional dependence on device parameters and terminal voltages was not specified.

This paper is organized as follows. In Sec. II we will present the full range analytic compact model for nano-MOSFETs according to scattering theory. In Sec. III a brief description of the model device used in this work is given. In Sec. IV various approach to calculate the approximate channel backscattering coefficient are briefly described. Section V compares analytical results with those obtained from 2D numerical simulation [4]. Finally, Sec. VI contains the summary and conclusions of this paper.

II. THEORY

According to scattering theory, carriers are injected from the source to the low field region at the beginning of the channel over source channel potential barrier as shown in Fig. 1. Some of the injected carriers backscatter in this low field region, which has length of ℓ. The length of this low field critical region is the distance over which the channel potential drops by approximately *kT/q* (hereafter called "*kT* layer") [2]. The carriers that cross this *kT* layer feel the high drain electric field, which acts as a absorber for the carriers and sweeps them towards the drain. Although the carriers scatter in the high field part of the channel, they cannot return to the source because of the field.

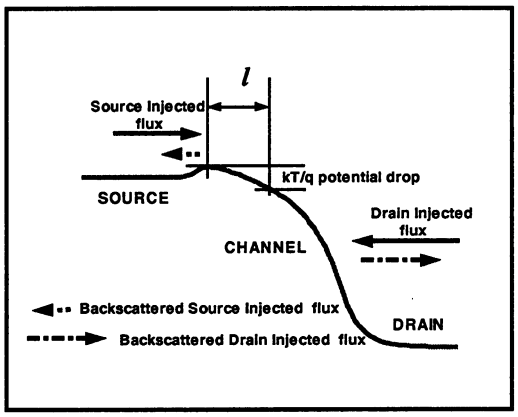

Fig. 1. Schematic representation of a nanoscale MOSFET according to scattering theory. The source and drain injected and backscattered fluxes and critical channel length are shown.

The charge at the beginning of the channel (the top of the potential barrier where field along the channel is zero) is controlled by the gate bias [5]. When the drain bias is low, the carrier distribution at this point assumes full-Maxwellian (or Fermi-Dirac) distribution in which negative velocity states are either injected from the drain or are backscattered by the channel. But when drain bias is high, the drain Fermi level is pulled down by drain bias and negative half of the distribution is cut off by the high drain to source potential barrier. Now at the beginning of the channel, negative going electrons are only those that are injected from the source and backscattered in the critical region "*kT* layer" at the beginning of the channel. Since only a fraction (*r*) of source-injected carriers are backscattered while rest go towards drain, there happens to be an imbalance in electrostatics at the beginning of the channel as the gate finds fewer charges at the beginning of the channel. This causes the conduction band to be pushed down relative to source Fermi level so that enough carriers can be injected from the source to maintain charge balance at the top of the barrier [5]. So the carrier

distribution at the top of the source channel barrier becomes asymmetrical with more positive-going carriers injected from the source while less negative-going carriers (those backscattered in the critical region). In the full ballistic case when there is no backscattering anywhere in the channel the carrier distribution at the beginning of the channel assumes a perfect hemi-Fermi-Dirac shape. As negative-going carriers are suppressed while the positive-going states are enhanced, the unidirectional thermal velocity at the beginning of the channel increases. Therefore, the maximum value of injection velocity is the thermal velocity of a hemi-Fermi-Dirac distribution.

Guided by the theory of nanoscale devices outlined above, we have derived a full-range scattering model assuming degenerate Fermi-Dirac carrier statistics. It expresses current in a MOSFET as a function of device width (W), drain bias, charge at the beginning of the channel $Q_n(0)$, and channel backscattering coefficient r.

$$I_{DS} = WQ_n(0)\left(\frac{1-r}{1+r}\right)\left[v_T \frac{\Im_{1/2}(\eta_F)}{\ln(1+e^{\eta_F})}\right] \times \left\{\frac{1-\dfrac{\Im_{1/2}(\eta_F - U_{DS})}{\Im_{1/2}(\eta_F)}}{1+\left(\dfrac{1-r}{1+r}\right)\dfrac{\ln(1+e^{\eta_F - U_{DS}})}{\ln(1+e^{\eta_F})}}\right\} . \quad (1)$$

To derive this equation, single sub-band conduction has been assumed, and $v_T = \sqrt{2k_BT/\pi m_t}$ is the unidirectional thermal velocity under non-degenerate condition. In eq. (1) the Fermi-Dirac integrals of order ½ and 0 in the square bracket containing v_T, account for the increase of v_T due to degeneracy. Hereafter, we will call this enhanced velocity as $\tilde{v}_T$. η_F and U_{DS} are the normalized Fermi level and drain bias respectively. When $r = 0$, we obtain a simple model for the ballistic MOSFET. Under high drain bias, the last factor is unity, and we obtain a simple expression for the on current [2]. With low drain bias, we find a finite conductance analogous to the well-known e^2/h quantum conductance [3]. The central problem in developing the scattering model lies in relating $r(V_{DS}, V_{GS})$ to the self-consistent channel potential and the scattering mechanisms within the channel. Two simple approaches to calculate r are briefly described in Sec. IV. In the present work, 1D electrostatics was used to find $Q_n(0)$ that is charge at the beginning of the channel.

III. DEVICE MODEL

A symmetric double-gate MOSFET with 20nm channel length is used as a model device in this paper. This device structure is thought to provide the best prospects for scaling channel lengths to the 10nm range [4], and its simple geometry facilitates the development of analytical models.

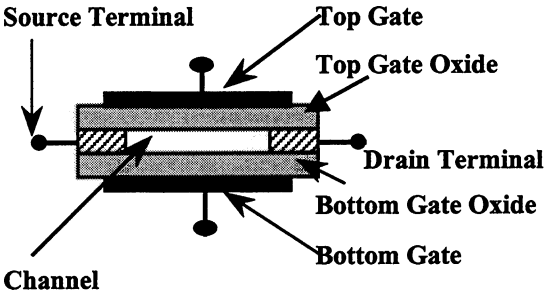

Figure 2. Schematic representation of device structure of a Double Gate MOSFET used in this paper.

The top and bottom gate oxide thickness are 1.5nm, which is assumed to be scaling limit of oxide thickness before excessive gate tunneling can be tolerated. The Si body thickness is taken as 1.5nm. The exceptionally thin body curb short channel effects for this 20nm channel length device. The channel doping is assumed to be zero. For this 1.5nm body thickness, only a single sub-band is occupied.

IV. ANALYTICAL EVALUATION OF r

In the case of full ballistic transport in the channel, the source-injected positive-going flux, crosses the channel and reaches drain without any backscattering, and $r = 0$. According to scattering theory, backscattering from the channel is determined only by a region of short length (ℓ) at the beginning of the channel. ℓ is the distance from the top of the barrier to the point where potential drops by kT/q volts. A simple expression that relates ℓ to r is [2]

$$r = \frac{\ell}{\ell + \lambda}, \quad (2)$$

where λ is the momentum relaxation length in this low field kT layer. It can be found by momentum relaxation time (from low field mobility at the beginning of the channel) and unidirectional thermal velocity $\tilde{v}_T$. When drain bias is less than kT/q, the physical channel length (L) replaces ℓ in eq. (2).

To get r from eq. (2), the critical length ℓ is needed. In principle, this has to be determined from the self-consistent channel potential profile. Numerical simulation provides a rigorous evaluation, but for an analytical model, we consider simple cases; collision-dominated and collision-free [6]. The collision-dominated channel potential profile was obtained by solving 1D Poission equation in which the charge

density was given by drift-diffusion transport with gradual channel approximation. The channel potential profile was found to vary as $x^{3/2}$, where x is the distance from the top of the source channel barrier. The second non-self-consistent channel potential profile was obtained by assuming collision-free transport in the channel, where it was found to vary with as $x^{4/3}$. In both cases, the length ℓ of the kT layer was extracted as a function of V_{DS}.

V. RESULT AND DISCUSSION

In this section, we will discuss the electrical characteristics of a 20nm DG MOSFET calculated by the compact model proposed in eq. 1. The results are compared with the 2D self-consistent numerical simulation of the same device [4].

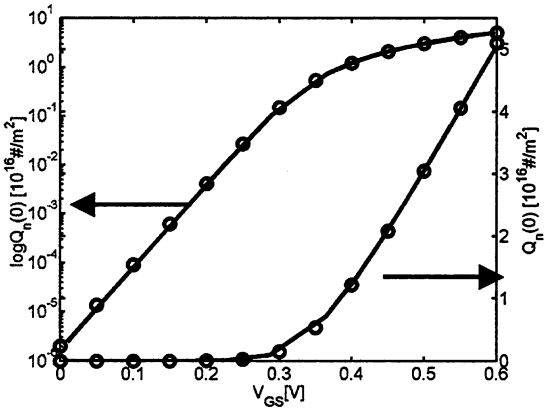

Figure 3. Analytically computed $Q_n(0)$ *vs.* V_{GS} (solid line) in equilibrium (V_{DS} = 0V) compared with 2D numerical simulation (circles).

Figure 3 shows log and linear scale charge density at the top of the source-channel barrier at zero drain bias. Although, one (circles) was computed by 2D self-consistent simulation and the other (solid) from analytical MOS-C 1D electrostatic analysis, the results are in good agreement both in sub-threshold and above threshold regions. In this 20nm device, the top of the barrier is the middle of the channel (at zero drain bias) where the diffused carriers from heavily doped (10^{20} /cm^3) source and drain are negligible, so 1D electrostatic analysis is valid. However, in shorter channel devices the diffused charge is not negligible at the top of the barrier, which is a limitation of 1D electrostatic analysis used here.

In Fig. 4, the simulated ballistic I_{DS} vs. V_{GS} results are given. It can be seen that the analytical compact model of eq. (1) shows good agreement with the corresponding numerical simulation. For this 20nm channel length device, body is thin (1.5nm) enough to curb 2D effects and so very small DIBL is seen between high (V_{DS} = 0.6V) and low (V_{DS} = 0.05V) drain bias conditions. The sub-threshold characteristics are almost ideal for both analytical and numerical results. The simple 1D MOS-C electrostatic analysis for $Q_n(0)$

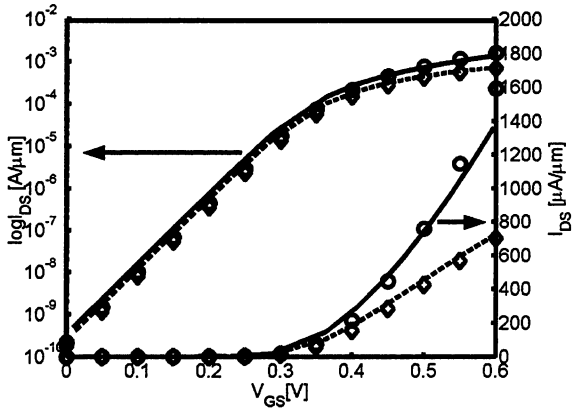

Figure 4. Linear and log plot of simulated ballistic (r = 0) I_{DS} vs. V_{GS} characteristics. The solid and dashed lines represent the results from present analytic model at high (V_{DS} = 0.6V) and low (V_{DS}= 0.05V) drain biases respectively. The corresponding results from numerical simulations are shown in circles and diamonds respectively.

used in the analytic model fails to capture the additional increase in charge density at the beginning of the channel at highest drain bias (V_{DS}= 0.6V). At high drain bias, the drain field lowers the source to channel barrier which increases the charge $Q_n(0)$ at the beginning of the channel. So there is a difference in on-currents in analytical and numerical ballistic results as seen in Fig. 4. A more sophisticated charge density model can remove this limitation.

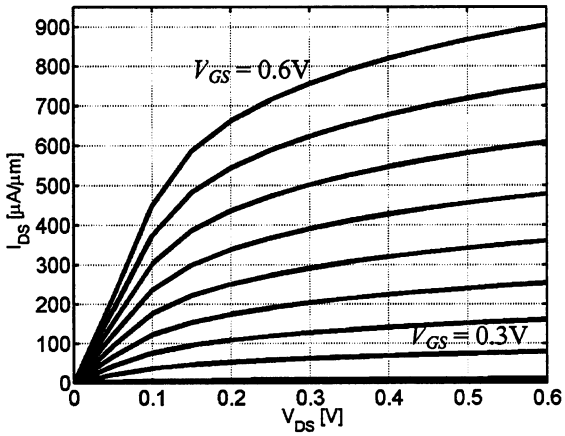

Figure 5. Computed I_{DS}-V_{DS} characteristics (with gate voltage as parameter) of a 20nm Double Gate MOSFET using the new full-range compact model. The drift diffusion approach was used compute ℓ for eq. (2). A low field mobility of 120 cm^2/V-sec was used to obtain λ, the momentum relaxation length.

In Fig. 5, the above threshold I_{DS} vs. V_{DS} characteristics for the present 20nm channel length DG MOSFET are shown with V_{GS} as parameter. Current is calculated using eq. (1) where the channel backscattering coefficient r is calculated assuming collision-dominated (drift-diffusion) transport in the channel as briefly described in Sec. IV. The value of low field mobility μ_n used in this simulation is 120 cm^2/V-sec.

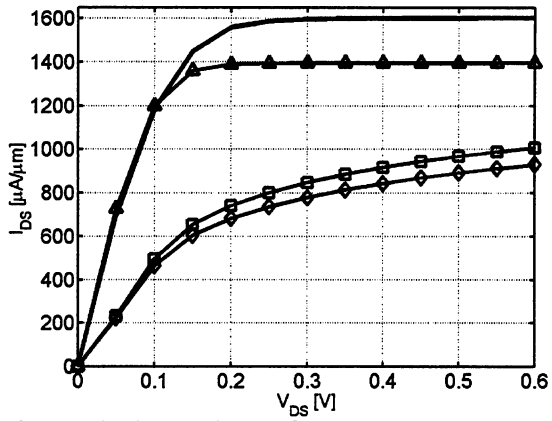

Figure 6. Comparison of I_{DS}-V_{DS} at maximum gate voltage (V_{GS} = 0.6V). Four cases are shown. Numerical ballistic (solid), analytical ballistic (triangle), analytical results ($r \neq 0$) based on drift-diffusion (diamond) and analytical results ($r \neq 0$) based on collision free transport (square).

In Fig. 6, the on currents are compared as obtained from different transport models. All results shown are at maximum gate bias (V_{GS} = 0.6V). The triangle markers show the ballistic result from eq. (1) with r = 0. The solid line is 2D numerical, self-consistent simulation of the same case. The difference in on currents (1600 μA/μm from numerical simulation and 1400 μA/μm from eq. (1) with r = 0) is the result of increased charge density at the beginning of the channel at high drain bias which is not captured in 1D electrostatic analysis used for $Q_n(0)$ in eq. (1). The square marked curve results from calculating channel backscattering coefficient r assuming collision-free transport in the channel. It does not imply full ballistic transport with r = 0. Here collision-free transport is assumed merely to approximate the potential profile along the channel so that r can be calculated using eq. (2). The diamond marked plot is obtained by calculating critical length ℓ using collision-dominated transport (drift-diffusion) in the channel. Both for collision-free and collision-dominated case, low field electron mobility of 120 cm^2/V-sec are used to calculate momentum relaxation length λ in eq. (2). It can be seen that both collision free and collision-dominated transport gives almost same maximum current. The results are consistent with scattering theory according to which the current drive of a MOSFET is rather insensitive to the detailed transport of carriers in the entire channel, while it critically depends on the length of first "kT layer" where collision determines the net reflection of the source-injected flux. Since the length of this layer, ℓ, does not vary much with the choice of transport model in the channel, the current becomes insensitive to the choice of transport model. Also it is shown in Fig. 6 that a 20nm DG MOSFET will operates at about 60% of the full ballistic limit of operation if the low field electron mobility is 120 cm^2/V-sec.

VI. SUMMARY AND CONCLUSION

In summary, we introduce a new approach to compact transistor modeling, one with roughly the complexity of a SPICE model but which is valid to the scaling limits of transistors. Different approaches to compute r, the key parameter in the model, are discussed and compared, and this analytical model is compared to detailed numerical simulations. To farther develop this prototype circuit model, several additional factors have to be addressed (e.g. 2D electrostatics and the influence of degenerate carrier statistics on the length ℓ). New models of this class can provide a useful conceptual guide for device development as well as circuit models for new, unconventional transistors.

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