3-D Simulation and Modeling of Signal Isolation in RF/IF Circuits

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ABSTRACT

In this paper, we present a practical methodolgy for the 3-dimensional simulation of signal isolation structures along with comparison to measurements made on test structures. We also describe the extraction of a scalable compact model for isolation structures. Such SPICE models are mandatory during the design process for predicting the effect of substrate noise generated by digital circuit blocks on highly sensitive low noise amplifiers in the RF and IF range.

Keywords: Signal isolation, compact modeling, substrate coupling, on-chip crosstalk.

1 INTRODUCTION

The future trend in systems on a chip is: (1) operation at higher frequencies and (2) integration of RF and digital applications on a common platform. Switching transients induced by digital circuit blocks can adversely effect the performance of analog components, which are sensitive to voltage variations of the substrate ground. The increase of the operating frequency in telecommunication chips raises the noise injection to a level that could compromise the performance of the circuit. Therefore the study of substrate coupling becomes more important and a big challenge for new RF-CMOS and BiCMOS technologies is the development of high quality signal isolation concepts.

Several approaches have been put forth to reduce substrate cross-talk as well as to analyze and model it[1-3]. Recent studies have demonstrated a potential advantage of standard SOI substrates over bulk silicon for crosstalk reduction, but only at frequencies up to about 1 GHz[4,5]. Later analyses have shown improved crosstalk reduction using junction isolation techniques[6,7]. Previous TCAD simulations[4] using 2-D modeling have shown that for the size of the structures considered for signal isolation, signal spreading in the third dimension is significant and requires accurate simulation. This paper considers two structures:
(1) p^+ guard rings completely enclosing a given region: They are grounded and provide isolation by /screening the substrate potential fluctuations generated by adjacent devices. A schematic cross-section is shown in figure 1. A variation of this scheme is to enclose both the source and the sensor with similar p^+ guard rings.
(2) a fully junction isolated p-well: the source pad and p-well are completely surrounded with n-type material. The schematic diagram for this isolation structure is given in figure 2.

2 3-D COMPUTER SIMULATIONS

The 3-D structures are constructed with doping profiles for Motorola's next generation BiCMOS process on a p^+ substrate. Figure 3 shows results from ISE's software MESH. The challenge of 3D meshing was solved through a re-gridding procedure. The Poisson equation is first solved for an initial very fine grid with ~100,000 grid points. The structure is then meshed based on the distribution of the electric field and the space charge to get a grid with reasonable resolution around junctions and 30,000 to 40,000 grid points.

2.1 AC Small Signal Analysis Based on Transient Analysis and Fourier Transform

The quality of signal isolation structures is usually tested by measuring the scattering parameter S21. Simulation of these parameters for such 3D structures with the standard method for small signal analysis[8] will lead to a rather high CPU time and memory consumption. We have therefore chosen to assess these parameters by means of transient simulations and subsequent Fourier transformations of the transient terminal voltages and currents. Figure 4 shows the graph of the voltage pulse used to excite the two contacts and the resulting current at the opposite contact. The ratio of the Fourier transform of the current at terminal m and the Fourier transform of the voltage at terminal n results in the Y-parameter Y(m,n).

$$Y(m,n)=\frac{I_m(\omega)}{V_n(\omega)} \tag{1}$$

Subsequent transformation into S-parameters is done using the equations given in [9]. In order for this to be accurate the following prerequisites need to be fulfilled: (1) The excitation voltage must be a small signal so that the prerequisite of small signal analysis is fulfilled. It is

typically sufficient to keep the absolute value below 0.1V. (2) The numerical error during transient time integration and Fourier transformation must be small, so that the discrete numerical approximation of the current after linear interpolation is in good agreement with the exact current. We have used a *fourier* routine from the GALENE III software package[10] which is exact for piece-wise linear time functions. Therefore the result should be sufficiently accurate as long as the discrete approximation of the time signal after linear interpolation is in good agreement with the exact time signal.

2.2 Results

The magnitude of the scattering parameter S21 is simulated for a DOE of more than 10 different device geometry parameters in the frequency range from 10 MHz to 100 GHz using the 3D device simulator DESSIS[11] along with the routine *fourier* from GALENE III. Fig. 4 shows the voltage signal used for the transient simulation together with a sample for the current response on the terminals a and c. All curves are discretized with non-uniform time steps. The minimum time step is 1e-18 s and the total number of time steps is ~150. Fig. 5 shows a set of Y-parameters resulting from this simulation as defined using equation (1). The S-parameters of test structures were measured using a HP8510C Network Analyzer and HP4142B Modular DC source. Simulation results are shown to be in good agreement with experimental measurements for a control space of test structures (figure 6). The results from this figure indicate that the guard ring structure improves the low frequency isolation by 20 dB while the isolated p-well structure improves it by 40 dB. The degree of isolation decreases with increasing frequency in all cases. Both isolation schemes are inefficient for frequencies above 10 GHz. Further improvement can now be studied by varying the process and layout outside of the control set. As an example we compare results for a further optimized isolation concept in figure 7. For this structure, the low frequency isolation is improved by about 60 dB over the isolated p-well case and the high frequency isolation by about 10 dB.

3 EQUIVALENT CIRCUIT

The use of a 3-dimensional simulator is impractical for the purposes of simulating the different isolation schemes in the presence of actual circuits Circuit simulators such as SPICE are better suited for this purpose. The 3-D structure is therefore reduced to a simple, physically based equivalent circuit consisting of a few elements. For the fully junction isolated substrate structure such an equivalent circuit is shown in figure 8. Values of the individual circuit elements are determined from appropriate 3-D sub-structures through AC small signal analysis. The values are then analytically correlated to the appropriate geometrical parameters. As an example this technique is described here for determining the values of the resistors R1, R2 and R3. The substructure represented is shown in figure 9. It consists of the source contact, a p^+ source pad to eliminate the capacitor C1, p-well and the well contact. The junction between the p-well and the n-type region is replaced by a contact **x**. The resistances between the electrodes **a**, **w** and **x** are determined using Y-parameters and then converted to R1, R2 and R3 using a $\Delta \leftrightarrow Y$ transformation. Similar substructures were chosen to determine the values of the remaining circuit elements as well. Fig. 8 contains examples for resulting equations that build the equivalent circuit. Fig. 10 shows good agreement between the actual measurements and the lumped element equivalent circuit for the scattering parameter S21. The calibrated compact model provided in this work can now be effectively used for further fine tuning of isolation structures and is a valuable tool for technology development.

4 CONCLUSIONS

A transient analysis technique in a 3-D device simulator has been used to model two different signal isolation schemes. Lumped element equivalent circuits are generated for the isolated p-well structures by modeling 3-D substructures. Good agreement has been demonstrated between the 3-D simulations, measurements and equivalent circuit simulations. The compact model thus extracted can be used to facilitate circuit design and layout at an early stage of the development process.

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REFERENCES

[1] K. Joardar, Proceedings of the 1995 Bipolar/BiCMOS Circuits and Technology Meeting, p.178, 1995.

[2] D. K. Su, M. J. Loinaz, S. Masui and B. A. Wooley, IEEE Journal of Solid-State Circuits, vol. 28 (4), p.420, 1993.

[3] A. Samavedam, A. Sadate, K. Mayaram and T. Fiez, IEEE Journal of Solid-State Circuits, vol. 35 (6), p.895, 2000.

[4] K. Joardar, IEEE Journal of Solid-State Circuits, vol. 29 (10), p.1212, 1994.

[5] I. Rahim, I. Lim, J. Foerstner and B. Y. Wang, Proc. IEEE Int. SOI Conf., 1992, p. 170.

[6] K. Joardar, Electron. Lett., no. 15, p. 1230, 1995.

[7] T. Riihisaari, H. Ronkainen and H. Hakojärvi, Proc. 28th European Solid-State Device Research Conf., p. 632, 1998.

[8] S. Laux, IEEE Trans. on Elec. Dev., ED-32(10), p. 2028, 1985.

[9] G. Gonzalez, Microwave Transistor Amplifiers: Analysis and Design, Prentice-Hall Inc., 1984.

[10] GALENE III, User Guide, University of Bremen, July 2000.

[11] DESSIS, ISE Integrated Systems Engineering AG, Zurich, Switzerland, ver. 6.0.5.

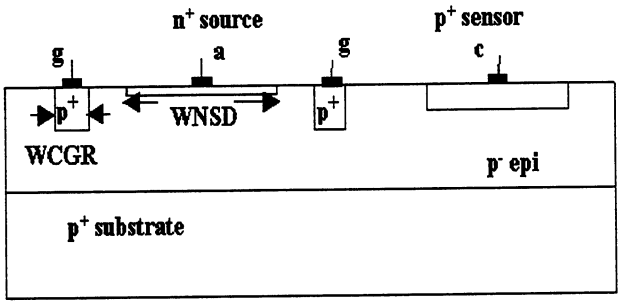


Figure 1: Schematic diagram of p^+ guard ring isolation structure

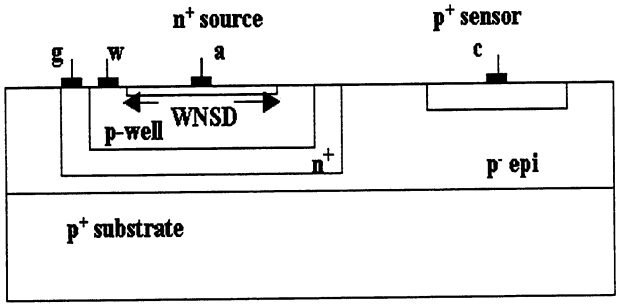


Figure 2: Schematic diagram of junction isolated p-well structure

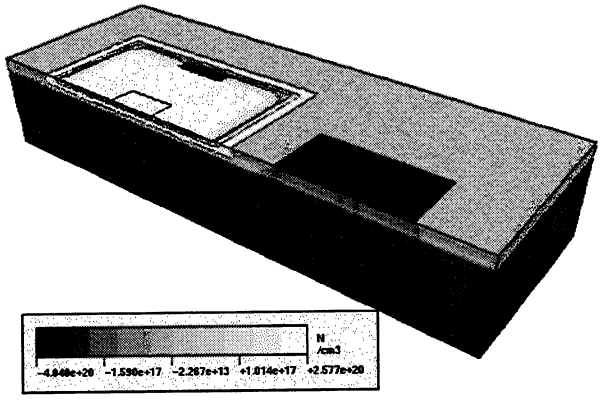


Figure 3a: 3-D image of guard ring isolation structure (~30,000 grid points)

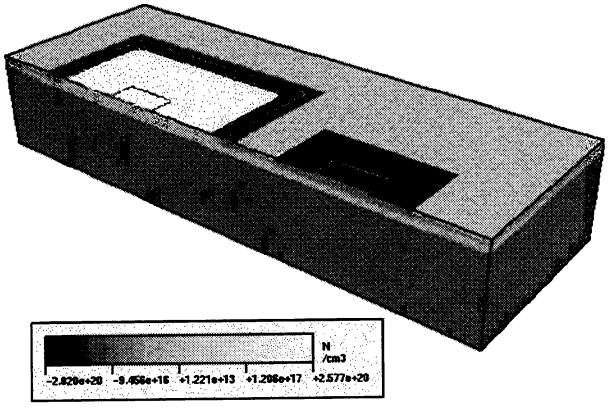


Figure 3b: 3-D image of junction isolated p-well structure (~40,000 grid points)

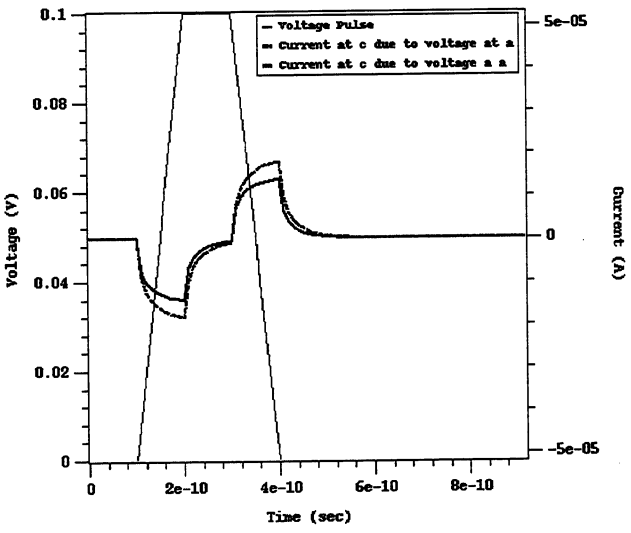


Figure 4: Graph of voltage pulse and resulting terminal currents vs. time

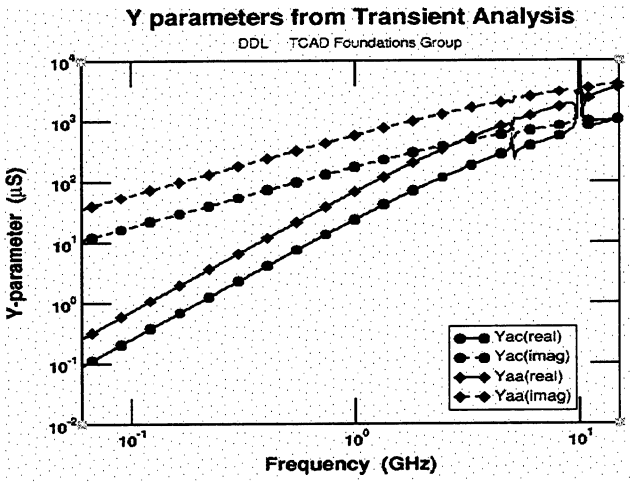


Figure 5: Y parameters extracted using transient analysis.

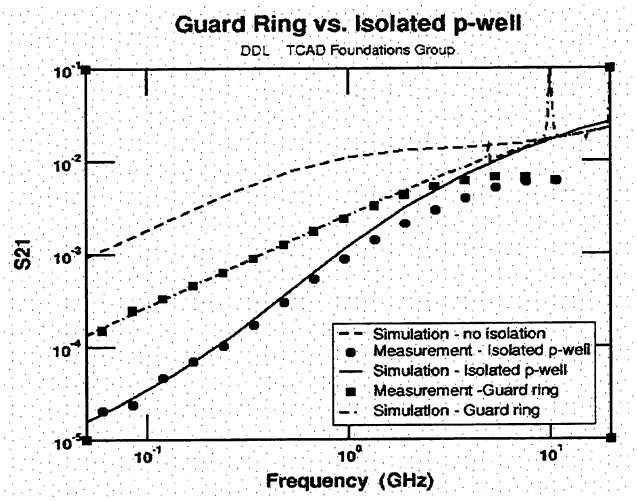


Figure 6: S21 comparison between guard ring and junction isolated structures.

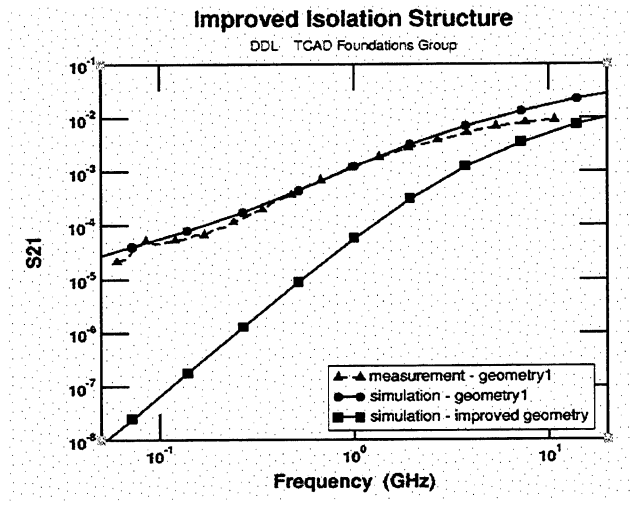
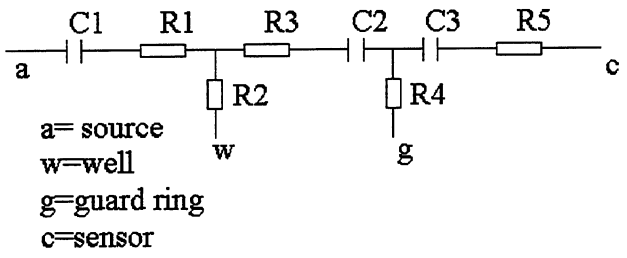


Figure 7: S21 comparison of single isolated p-well structure with an improved geometry structure.



$C1 = 6.49e\text{-}16*WNSD + 7.79e\text{-}16*(WNSD)^2$

$R5 = 88.5 - 0.325*SGR + 0.07*WNSD - 0.004*(WNSD)^2$

Figure 8: Equivalent circuit for compact model of isolated p-well structure along with sample equations for the circuit elements.

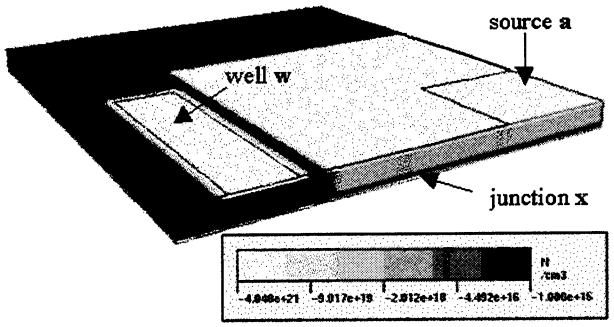


Figure 9: 3-D Substructure used for determining the values of the equivalent circuit parameters R1, R2 and R3.

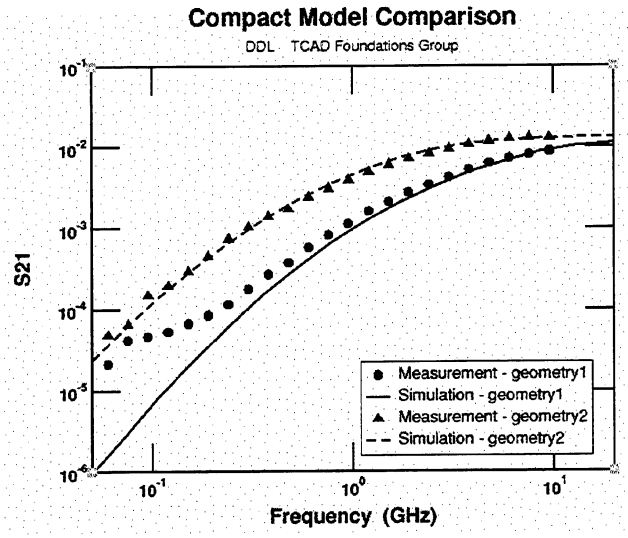


Figure 10: S21 comparison from compact model simulation and measurement for two different geometries.