A New Compact Model of Floating Gate Non-Volatile Memory Cells

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ABSTRACT

This paper presents a new compact model of Floating Gate Non-Volatile Memory Cells using SPICE circuit elements. It features many advantages compared to previous models: it is simple and easy to implement and to update, scalable, and its computational time is not critical, thus making it very attractive to industry. It is based on a new procedure which estimates the floating gate voltage without using fixed capacitive coupling coefficients, thus improving its simulation capability. Moreover, since this model requires only standard parameters extracted for SPICE-like models of MOS transistors (plus the floating gate to control gate capacitance), any industry CMOS parameter extraction procedure should be applied to the dummy cell (where the control gate and the floating gate are short-circuited). This model can be easily used both in device optimization and in circuit performance evaluation.

Keywords: Device and Circuit Simulation, Floating Gate devices, Nonvolatile Memories

1 INTRODUCTION

The modeling of Floating Gate (FG) memory cells is a well-known subject in the literature [1], even if few of the models proposed can be implemented in circuit simulators [2]. Generally, they are based on the "classic" lumped element description of the FG cell shown in Fig.1. Since the exact knowledge of FG voltage, V_{FG}, is required for the correct modeling of memory operations, these models calculate it through capacitive coupling coefficients ($\alpha_j = C_j/C_{TOT}$; where j = S, D, B, CG and $C_{TOT}=C_S+C_D+C_B+C_{CG}$, see Fig.1) [1], [3].

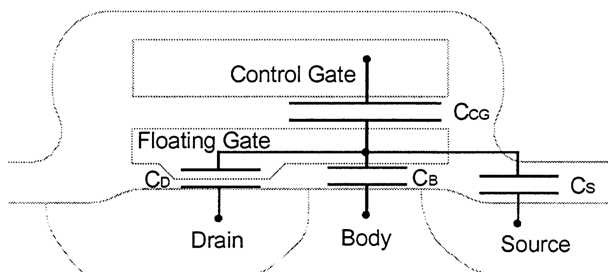

Figure 1. "Classic" model of FG memory cell based on a lumped element description: FG Voltage is calculated from a capacitive network.

However, these coefficients are not easy to measure, as the FG node cannot be directly accessed direct and indirect measurement techniques have been proposed [1], but in any case they require complex measurement procedures. Moreover, they depend on the applied terminal voltages [4], and therefore, considering them constant, as usually done, introduces errors. To overcome this limit, in our model the FG potential has been evaluated through a new calculation procedure, which does not use fixed capacitive coefficients, thus resulting in a more accurate estimate. Moreover, while the majority of the circuit models are mainly dedicated to highlight some physical phenomena within the complex functionality of the cell [5][6][7], this new model is able to reproduce the whole electrical-physical behavior of the memory cell. Since it is has been developed in a Spice-like ambient, it can be used not only to reproduce the single device, but also in circuit simulations: for example, the set of circuits devoted to sense the information stored in the cell, usually called read path.

2 THE MODEL

As shown in Fig.2 considering the case of a E^2PROM cell, this model is composed by four elements: a MOS transistor whose Source, Body, Drain are S, B, D, of the

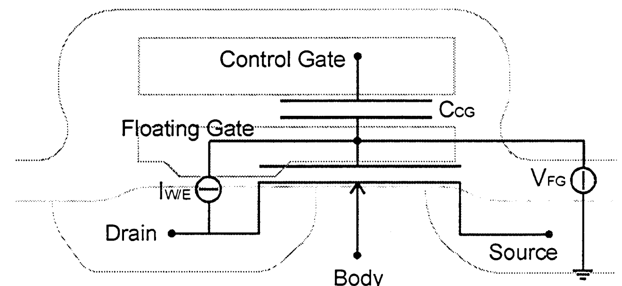

Figure 2. New model of FG memory cell. FG voltage is calculated from charge balance equations. Program/Erase current generators may be included, as well.

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cell, and Gate is the FG of the cell; a capacitor connected between FG and Control Gate; a voltage-controlled voltage source, V_{FG}, between FG and ground, to overcome the problem of simulating a capacitive net in DC conditions; a voltage-controlled current source, $I_{W/E}$, connected between FG and D, to reproduce write/erase currents, which for a E^2PROM cell are the well-known Fowler-Nordheim currents across the tunnel oxide between D and FG.

In the case of a Flash cell, since the physical phenomena underlying the write of these devices are different, we can either add some current sources or modify the existing ones to include program mechanisms like Channel Hot Electron and CHISEL [8]. Particularly, it is worth noting that this can be done independently of the other parts of the model, thus improving the update capability of the model.

The calculation of the FG potential is performed by a new procedure implemented in a C code routine, which solves the charge balance equation at the FG node. That is, the charge on the MOS gate, Q_G, is equal to the charge of the capacitor between the FG and CG, plus the charge forced in/out the floating gate during cell program/erase operations, Q_{FG}, which in DC condition is a constant and depends on the state of the cell.

$$Q_G(V_{FG}, V_S, V_D, V_B) = C_{CG}(V_{CG} - V_{FG}) + Q_{FG} \quad (1)$$

Q_G is a very complex analytical function of S, D, B and FG biases (V_S, V_D, V_B and V_{CG}, respectively), which has been evaluated from the charge equations of the compact MOS transistor model adopted. To check that the physical meaning would not be lost, we have directly verified that (1) gives always a unique solution for the FG voltage, which is its only unknown term. In fact, the charge balance equation (1) is monotone versus V_{FG} for the all the combinations of V_S, V_D, V_B and V_{CG} of interest.

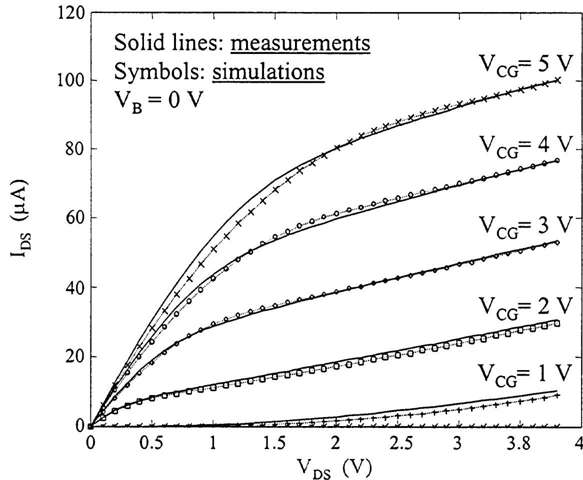

Figure 3. I_D-V_D characteristics measured (solid lines) and simulated (symbols) on an E^2PROM cell (W=0.3μm, L=0.75μm) varying the control gate voltage.

2.1 Advantages

The procedure just described represents the core of this model, which features new great advantages compared to previous ones [3], [7]. 1) It is very simple to implement, since it uses standard circuit elements whose parameters can be determined by applying a standard MOS parameter extraction procedure to the dummy cell (FG and Control Gate are short-circuited). The only additional parameter is the capacitance between FG and CG, C_{CG}, which can be extracted from the cell cross section.

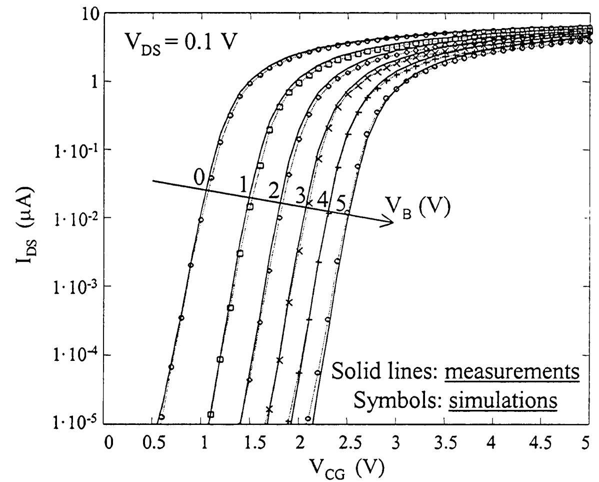

Figure 4. Subthreshold trans-characteristics measured (solid lines) and simulated (symbols) on a E^2PROM cell (W=0.3μm, L=0.75μm) varying the body voltage.

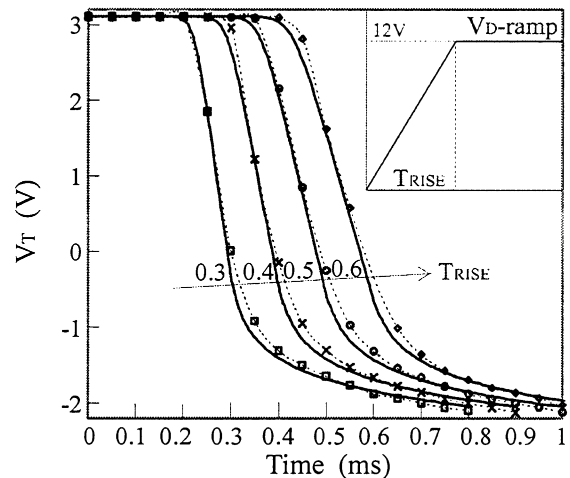

Figure 5. Measured (solid lines) and simulated (symbols) threshold voltage shift during write transients (V_{CB}=V_B=0, S floating) with different V_D ramp rise time.

2) This model is easily scalable, since the compact MOS model already takes the scaling rules into account and

they do not influence V_{FG} calculation procedure. 3) The write/erase current source can be changed independently of the other parts of the model, thus enabling future development in any analytical description of W/E mechanisms. 4) The accuracy of the model depends on the compact MOS model adopted, thus taking advantage of the many efforts put to improve and scale the MOS compact models.

3 RESULTS

The model described above has been applied on E^2PROM and Flash memory cells manufactured in 0.25μm technology. In Figs.3-5 the fitting capabilities of this model are shown compared to experimental data for an E^2PROM cell with W=0.3μm, L=0.75μm and C_{GC}=3fF.

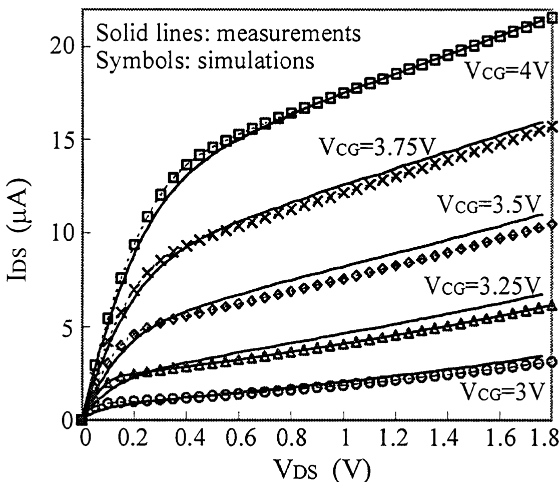

Figure 6. I_D-V_D characteristics measured (solid lines) and simulated (symbols) on a Flash cell (W=0.25μm, L=0.375μm) varying the control gate voltage.

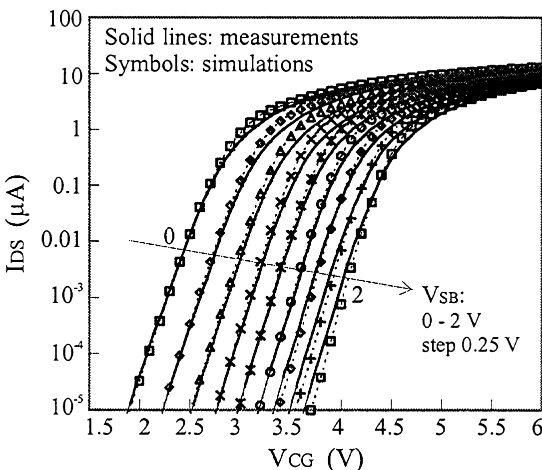

Figure 7. Subthreshold trans-characteristics measured (solid lines) and simulated (symbols) on a Flash cell (W=0.25μm, L=0.375μm) varying the body voltage.

Simulations reported in Figs. 3-5 have been obtained by assuming a small fixed charge in the floating gate (Q_{FG}=-0.65 fC), which is probably due to residual charge after W/E cycling. Instead, the initial charge present on the FG of the erased (written) cell has been evaluated comparing measurements and simulations of the initial threshold voltage. As shown in these figures, the agreement between I-V measurements and simulations is excellent in both DC (Figs.3-4) and transient (Fig.5) conditions, and no free parameters are necessary to improve the fitting quality.

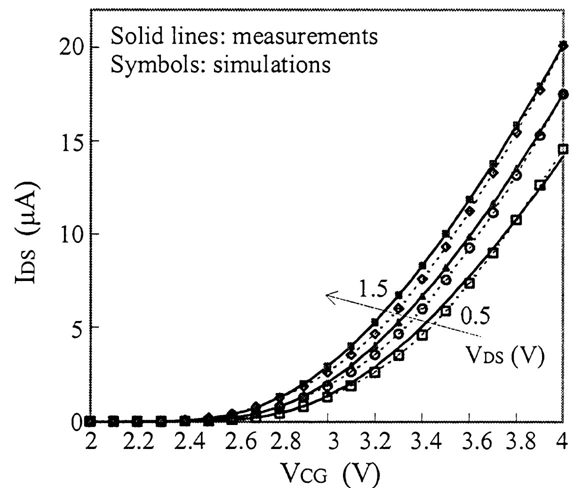

Figure 8. I_D-V_{CG} trans-characteristics measured (solid lines) and simulated (symbols) on a Flash cell (W=0.25μm, L=0.375μm) varying the voltage.

It is worth pointing out that two different approaches have been followed to model the real E^2PROM cell. In fact, since it is constituted by the series of the FG device and the select transistors, the contribution of this last ones should be included. This can be done directly by putting the select transistor Spice-like model in series with the one of the FG device, with the drawbacks that one additional model-cards has to be extracted and the implementation time become too large. Alternatively, since the gate of the select transistor is biased at 15 V when the memory cell is addressed, the select transistor contribution can be modeled approximately by a small increase of the drain resistance of the "dummy" transistor. Results obtained in the two cases are very similar; therefore the second approach has been preferred, as it requires only the extraction of one model-card (dummy cell).

In the case of Flash memory cells, this is not an issue, since the cell is composed by the single FG device. Again, in Figs.6-8, the agreement between simulation and measurements on a Flash cell (W=0.25μm, L=0.375μm and C_{GC}=0.8fF) is excellent in every possible bias combination, above and sub-threshold, with and without substrate bias. The compact MOS model assumed is Philips MM9 in both cases.

Moreover, this model describes correctly the W and L scaling of the cell. For example, Figs. 9-10 show the trends of the measured and simulated threshold voltage, V_T, which is the CG voltage that allows I_D=1μA/1μm channel width, when V_{DS}=0.1V. Measured V_T tends to increase with L and stays almost constant with W. Small variations are due to change in the initial charge in the FG of the measured samples. To highlight the theoretical behavior of the threshold voltage versus W and L, simulations depicted in Figs.9-10 have been performed assuming a constant charge density on the FG. As we have directly verified, Q_{FG} can be changed to improve the fitting and make the discrepancy between simulations and measurements to disappear.

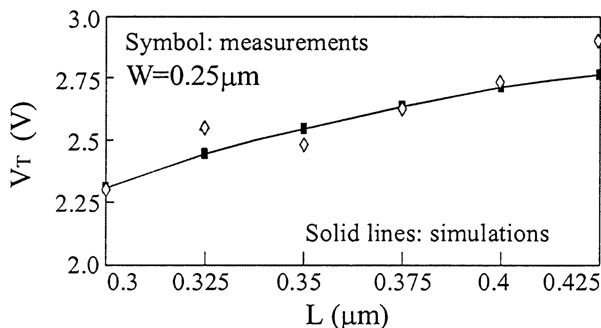

Figure 9. Comparison between the scaling L trends of threshold voltage measured (symbols) and simulated (solid lines) by keeping constant the FG charge density.

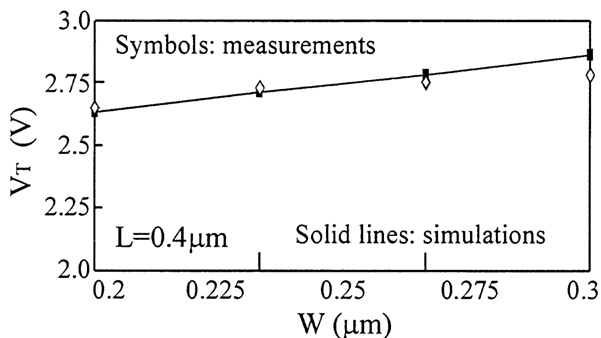

Figure 10. Comparison between the scaling W trends of threshold voltage measured (symbols) and simulated (solid lines) by keeping constant the FG charge density.

We have also used this model to simulate read-path circuits. Standard industry procedure substitutes the reference cell of the sense amplifier with a MOS transistor with adjusted V_T, and the cell to be sensed is a MOS transistor with high/low V_T depending on its state. We have used this complete model with a different value of Q_{FG} depending on the state of the memory cell and compared results. The main difference is in the rise time of the comparator output, which is a little slow down due to the more accurate capacitive load given by this new model. The simulation time is comparable.

4 CONCLUSIONS

The new Spice-like model of a FG memory cell we have developed is able to reproduce effectively the electrical behavior of E^2PROM and Flash cells in both DC and transient conditions. This model is based on a new procedure that permits to evaluate more accurately the FG potential without using fixed capacitive coupling coefficients. Moreover, it is scalable and simple to implement and to upgrade, its computation time is negligible and the parameter extraction procedure is the same used for a MOS transistor. The agreement with the experimental curves has been excellent without any free parameter to adjust the fitting quality in both E^2PROM and Flash cases. Its foundation on basic charge equation of the device allows also to use it as a tool for the analysis of results obtained with the "classic" models.

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