Compact Modeling of Avalanche Breakdown in pn-Junctions for Computer-Aided ESD Design (CAD for ESD)

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ABSTRACT

This paper presents and validates compact, physically-based electrothermal models of the avalanche process in pn junctions for use in network simulators (e.g Saber). Self-heating effects are also included. This enables the simulation of large systems of interconnected ESD structures, permitting a 'CAD-for-ESD' approach in commercial ESD design.

Keywords: Avalanche, breakdown, pn junction, ESD, CAD.

1 INTRODUCTION

Pn-junctions are a class of ESD structures that may typically undergo avalanche multiplication during an ESD pulse. ESD design requires consideration of the electrical as well as the coupled thermal behavior of the ESD structures being used. In industry-standard SPICE diode models, breakdown is represented by the linear combination of a DC term and an inverse-Shockley term (Fig. 1). While this SPICE representation is able to produce breakdown characteristics at room temperature (Fig. 2), the absence of the physics of the avalanche process causes the temperature coefficient of breakdown voltage to be incorrect in both sign and magnitude, as shown in Fig. 2. Consequently, SPICE diode models are unsuitable for the inclusion of self-heating or other higher-order electrothermal effects. In this paper, compact, physically-based temperature-dependent models of the avalanche process in one-sided pn junctions are presented. They have been implemented in Saber and validated using a 1N5368 diode. Self-heating effects have also been included and validated.

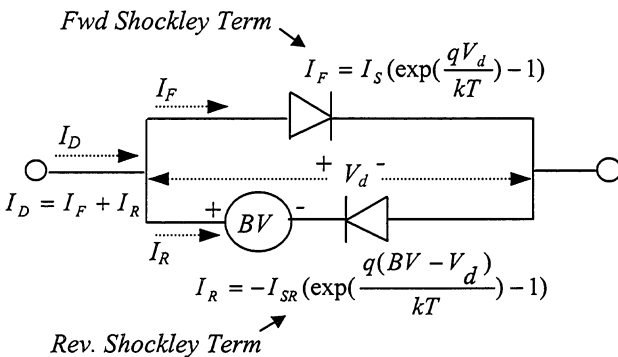


Figure 1: SPICE Diode Model, including breakdown

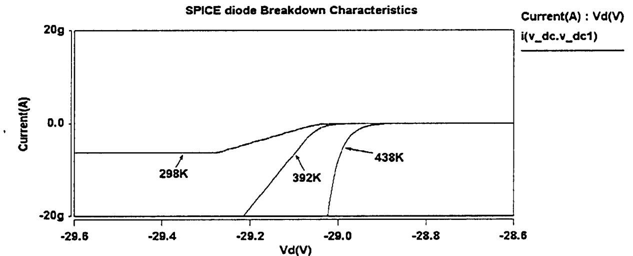


Figure 2: SPICE Diode Breakdown Characteristics as a function of Temperature.

2 ELECTRICAL MODEL

In this section, the models for the basic temperature-dependent electrical behavior of one-sided pn junctions(p^+n and n^+p) during avalanche breakdown are derived. Issues involved in their implementation in Saber are considered. Model validation using a 1N5368 diode is also shown.

2.1 Derivation

Consider a reverse-biased p^+n junction diode during avalanche breakdown. The one-dimensional differential equation relating hole current $J_p(x)$ to the rate of electron-hole pair generation in the junction is given by[1]:

$$\frac{dJ_p(x)}{dx} = \alpha_p(x)J_p(x) + \alpha_n(x)(J - J_p(x)), \tag{1}$$

where

$\alpha_p(x)$ is the impact ionization rate for holes,
$\alpha_n(x)$ is the impact ionization rate for electrons, and
J is the total current density (constant) in the junction.

$\alpha_p(x)$ and $\alpha_n(x)$ are given by[1]:

$$\alpha_p(x) = A_p \exp(-B_p / E(x)), \tag{2}$$

$$\alpha_n(x) = A_n \exp(-B_n / E(x)), \tag{3}$$

where $E(x)$ is the electric field in the junction and A_p, A_n, B_p and B_n are temperature-dependent[1] constants given by(for Si):

$$A_p = 2.25\times10^7 cm^{-1},\ A_n = 3.8\times10^6 cm^{-1},$$

$$B_p = 3.26\times10^6\left(\frac{T}{300}\right)^{0.2} cm^{-1},$$

$$B_n = 1.75\times10^6\left(\frac{T}{300}\right)^{0.2} cm^{-1}.$$

The solution of Eq. (1) yields the following expression for $J_p(x)$ (assuming that x=0 and x=W correspond to the edges of the junction in the n-region and the p-region respectively):

$$J_p(x) = \frac{\int_0^x \alpha_n J \exp(\int_0^{x'}(\alpha_n - \alpha_p)dx'')dx' + J_p(0)}{\exp(\int_0^x(\alpha_n - \alpha_p)dx')}. \quad (4)$$

Hence,

$$J_p(W) = \frac{\int_0^W \alpha_n J \exp(\int_0^{x'}(\alpha_n - \alpha_p)dx'')dx' + J_p(0)}{\exp(\int_0^W(\alpha_n - \alpha_p)dx')}. \quad (5)$$

Equation (9) may be rewritten in terms of the multiplication factor for holes, M_p, if it is assumed that electrons contribute negligibly to total current at the edge of the junction in the P^+ region, i.e.,

$$M_p = \frac{J_p(W)}{J_p(0)} \cong \frac{J}{J_p(0)} = \frac{1}{T_{p1}(W) - T_{p2}(W)}, \quad (6)$$

where

$$T_{p1}(W) = \exp(\int_0^W(\alpha_n - \alpha_p)dx), \quad (7)$$

$$T_{p2}(W) = \int_0^W \alpha_n \exp(\int_0^x(\alpha_n - \alpha_p)dx')dx. \quad (8)$$

$Jp(0)$ as well as W may be calculated from the applied voltage V_d using the standard equations for reverse-biased pn junctions [1]:

$$J_p(0) \cong J_{SR} = qn_i^2\left(\frac{1}{N_d}\sqrt{\frac{D_p}{\tau_p}} + \frac{1}{N_a}\sqrt{\frac{D_n}{\tau_n}}\right), \quad (9)$$

where J_{SR} is the reverse saturation current of the pn junction, n_i is the temperature-dependent intrinsic carrier concentration, calculated from the density of states in the conduction (N_C) and valence (N_V) bands, the material bandgap Eg, and temperature T as:

$$n_i = \sqrt{N_C N_V}\exp(-\frac{Eg}{2kT}),$$

D_p and D_n are the diffusion coefficients for holes and electrons respectively, and τ_n and τ_p are the electron and hole lifetimes.

$$W = \sqrt{\frac{\left(2\varepsilon V_{bi} - \left(V_d - \frac{JA}{G}\right)\right)}{q}\left(\frac{Na + Nd}{N_a N_d}\right)}, \quad (10)$$

where

the junction built-in potential is

$$V_{bi} = \frac{kT}{q}\ln\left(\frac{NaNd}{Na + Nd}\right),$$

N_a and N_d are the n- and p- doping concentrations,

ε is the permittivity of the material,

q is the electronic charge, 1.602×10^{-19}C,

A is the area of the junction, and

G is the effective conductance of the n- and p- bulk regions (assuming that Wn and Wp are their respective effective widths) :

$$G = \frac{q^2 A}{kT}\left(\frac{D_n N_d}{W_n} + \frac{D_p N_a}{W_p}\right). \quad (11)$$

Equations (6)-(11) and (2)-(3) represent avalanche breakdown in a P^+N junction, assuming that the electric field $E(x)$ in Eqs. (2)-(3) can be represented in a piecewise linear fashion, as shown in figure 3.

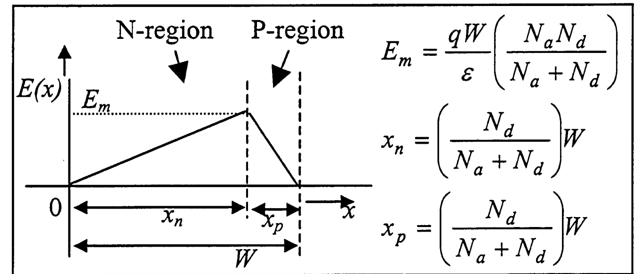


Figure 3: Piecewise Linear profile assumed for $E(x)$ (Eqs.(2)-(3)) in the p^+m as well as n^+p cases.

For an n^+p junction, the equations for avalanche breakdown may be derived in an analogous fashion, starting from the differential equation for electron current $J_n(x)$ in the junction during breakdown:

$$\frac{dJ_n(x)}{dx} = -\alpha_n(x)J_n(x) + \alpha_p(x)(J_n(x) - J) \quad (12)$$

[1] The temperature dependencies of B_p and B_n are empirical and have been developed by the authors so that the best possible fit to Fig. 32 in [1] is obtained. The temperature dependencies of A_p, and A_n, are being neglected.

The solution of Eq. (12) yields (again assuming that $x=0$ and $x=W$ correspond to the edges of the junctions in the n-region and p-region respectively):

$$J_n(x) = \frac{\int_x^W \alpha_p J \exp(\int_{x'}^W (\alpha_p - \alpha_n)dx'')dx' + J_n(W)}{\exp(\int_x^W (\alpha_p - \alpha_n)dx')} . \quad (13)$$

Hence,

$$J_n(0) = \frac{\int_0^W \alpha_p J \exp(\int_{x'}^W (\alpha_p - \alpha_n)dx'')dx' + J_n(W)}{\exp(\int_0^W (\alpha_p - \alpha_n)dx')} . \quad (14)$$

Eq. (14) can be rewritten in terms of the multiplication factor for electrons, M_n, as:

$$M_n = \frac{J_n(0)}{J_n(W)} \cong \frac{J}{J_n(W)} = \frac{1}{T_{n1}(W) - T_{n2}(W)} . \quad (15)$$

where

$$T_{n1}(W) = \exp(\int_0^W (\alpha_p - \alpha_n)dx) , \quad (16)$$

$$T_{n2}(W) = \int_0^W \alpha_p \exp(\int_{x'}^W (\alpha_p - \alpha_n)dx')dx . \quad (17)$$

W is calculated from the reverse voltage V_d using (10). As in (9), we assume:

$$J_n(0) \cong J_{SR} = qn_i^2 \left(\frac{1}{N_d}\sqrt{\frac{D_p}{\tau_p}} + \frac{1}{N_a}\sqrt{\frac{D_n}{\tau_n}} \right) . \quad (18)$$

Equations (15)-(18), (10) and (2)-(3) represent avalanche breakdown in an n$^+$p junction. As with the p$^+$n case, the electric field $E(x)$ in eqs. (2)-(3) is assumed to have the piecewise linear profile shown in figure 3.

2.2 Saber Implementation

The main issue involved in implementing the above p$^+$n and n$^+$p models in Saber is the numerical evaluation of $T_{p1}(W)$, $T_{p2}(W)$, $T_{n1}(W)$ and $T_{n2}(W)$ (eqs (13)-(14) and (23)-(24)), since a numerical integration program is unavailable. The above models were successfully implemented in Saber by using the first several[2] terms of Taylor Series expansions of the integrands about points that yielded a convergent sequence of terms.

For a p$^+$n diode, $x_p \cong 0$, $x_n \cong W$ and (see figure 3):

$$E(x) = \frac{E_m x}{W} = \frac{q}{\varepsilon}\left(\frac{N_a N_d}{N_a + N_d}\right)x . \quad (19)$$

[2] In the implementation of T_{p1} and T_{n1}, the first 8 terms were used, while for T_{p2} and T_{n2}, the first 4 terms were used

Likewise, for a n$^+$p diode, $x_n \cong 0$, $x_p \cong W$ and

$$E(x) = \frac{E_m x}{W} = \frac{q}{\varepsilon}\left(\frac{N_a N_d}{N_a + N_d}\right)x . \quad (19)$$

The analytical 'series-forms' for $T_{p1}(W)$ (Eq. (7)) and $T_{n1}(W)$ (Eq. (16)) may be derived by expanding their integrands about $x=W$ and $x=0$ respectively

$$T_{p1}(W) = \exp\left(\int_0^W dx \sum_{i=1}^{\infty} \frac{(x-W)^i}{i!} \frac{d^i(\alpha_n(x) - \alpha_p(x))}{dx^i}\bigg|_{x=W} \right), \quad (21)$$

$$T_{n1}(W) = \exp\left(\int_0^W dx \sum_{i=1}^{\infty} \frac{x^i}{i!} \frac{d^i(\alpha_p(x) - \alpha_n(x))}{dx^i}\bigg|_{x=0} \right) \quad (22)$$

The analytical series-forms for $T_{p2}(W)$ (Eq. (8)) and $T_{n2}(W)$ (Eq. (9)) may be derived by expanding their integrands about $x=W$ and $x=0$ respectively:

$$T_{p2}(W) = \int_0^W dx \sum_{i=1}^{\infty} \frac{(x-W)^i}{i!} \frac{d^i(\alpha_p(x)T_{p1}(x))}{dx^i}\bigg|_{x=W} , \quad (33)$$

$$T_{n2}(W) = \int_0^W dx \sum_{i=1}^{\infty} \frac{x^i}{i!} \frac{d^i(\alpha_n(x)(T_{n1}(W) - T_{n1}(x))}{dx^i}\bigg|_{x=0} \quad (33)$$

It is noted that Eqs. (21) and (23) (p$^+$n case), Eq. (19) use the analytical forms (using Eq.(2) and Eq.(3)) of $\alpha_n(x)$ and $\alpha_p(x)$ derived from (19), while Eqs. (22) and (24) (n$^+$p case) use Eq.(20).

2.3 Validation and System Simulation

A 1N5368 diode was used for validation. Figures 4 and 5 show the corresponding simulation and measured characteristics.

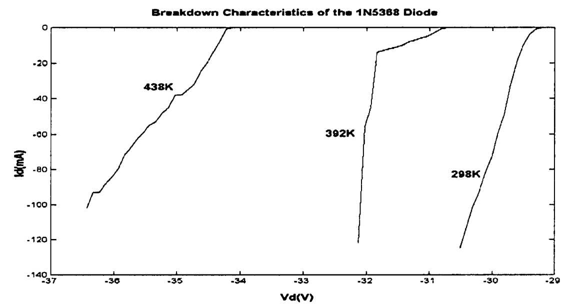


Figure 4: Temperature dependent breakdown characteristics of a 1N5368 diode.

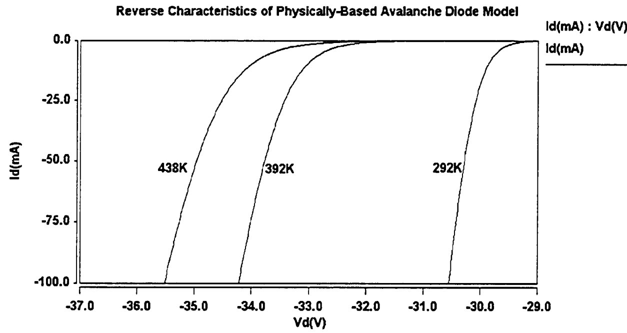


Figure 5: Saber simulation of the 1N5368 model.

3 THERMAL (SELF-HEATING) MODEL

To demonstrate the simulation of dynamic electrothermal behavior in ESD systems, the self-heating model for the 1N5368 diode has been developed and validated. As shown in figure 6, the self-heating model is a thermal subcircuit comprising of thermal resistive and capacitive elements.

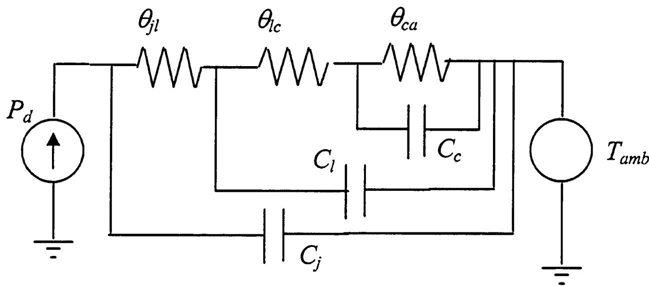


Figure 6: Self-Heating (Thermal) Subcircuit Model.

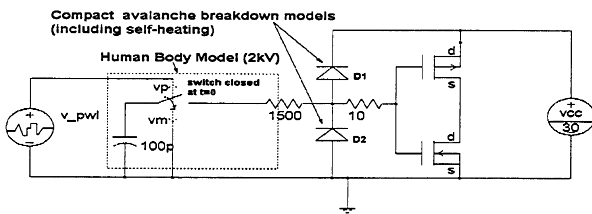
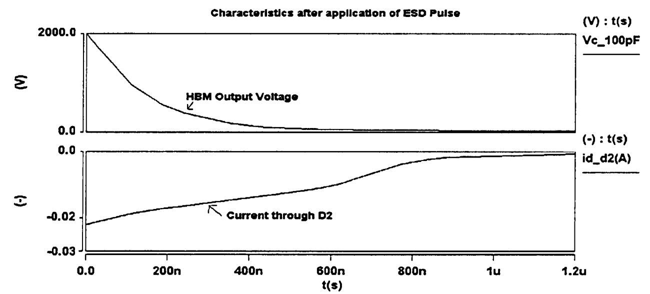


Figure 7: Inverter with dual-diode ESD protection at the gate being subjected to a 2kV HBM ESD pulse.

Figure 8 shows the output of the simulation of the circuit in figure 7 with self-heating included in the diodes. The diode D2 undergoes avalanche breakdown upon application of the ESD pulse. The junction temperature for D2(t_j) is shown which provides quantitative information on how well D2 will survive the ESD pulse.



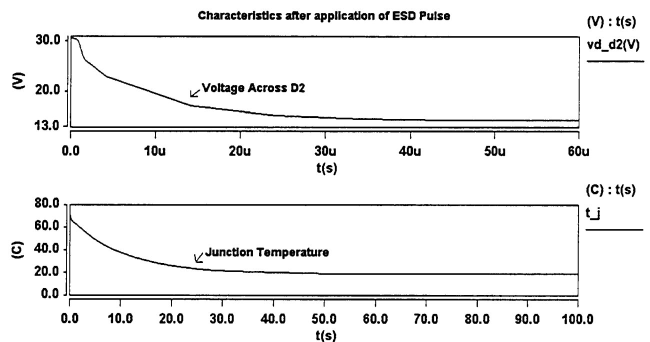


Figure 8: Post-ESD simulation results for the circuit in Fig. 7. Note the timescale difference for junction temperature.

4 CONCLUSIONS

Compact, physically based, temperature dependent models for avalanche breakdown in one-sided pn-junctions have been developed and validated using a 1N5368 diode. The models produce the expected I-V relationship (including the theoretical 'breakdown knee') as well as the correct sign and magnitude of the temperature coefficient of breakdown voltage. An example Saber model for the thermal circuit in the 1N5368 diode has also been developed and validated. Coupled simulations of the validated temperature dependent models and the thermal model have been used to successfully simulate an ESD pulse in an example circuit, demonstrating their suitability for use in 'CAD for ESD' applications.

REFERENCES

[1] Sze, S.M., "Physics of Semiconductor Devices," John Wiley, 1981.