

Towards Predictable TCAD

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ABSTRACT

This paper gives an overview of the status of technology computer-aided design (TCAD) as it is used today for research, development and manufacturing projects in the micro- and opto-electronics industry. While the accurate and physics-based simulation of process steps for ultra-scaled silicon technologies is still an area of active research, the simulation of electrical and optical effects has reached a high level of maturity for both Si and non-Si devices.

Keywords: Technology CAD, predictive modeling, process simulation, device simulation, manufacturing CAD

1 INTRODUCTION TO THE TCAD SIMULATION HIERARCHY

Over the past decade, the exploitation of advanced software tools has become standard practice in the micro- and, for certain applications, even in the opto-electronics industry. In this contribution, I try to give an overview of the status of numerical simulation in process and device research, development and manufacturing. As a result of the excellent progress in areas such as process and device physics, the utilization of experimental techniques for model calibration and the power of modern scientific computing, our understanding of the enormous advantages and possible limitations of TCAD has reached a level that was considered not possible only a few years ago. Aided by the PC revolution, this has completely changed today.

The different levels of the TCAD hierarchy are summarized in Fig. 1. At the lowest level, *process simulation* involves the modeling of the individual fabrication steps in a process, including all thermal and doping steps (i.e. ion implantation, rapid thermal annealing, epitaxy, and oxidation) as well as all pattern definition (i.e. lithography) and pattern transfer (i.e. etching, deposition) steps. From the simulation viewpoint, the calculation of highly accurate impurity distributions is of foremost interest. While the modeling of ion implantation and thermal processing has a history as long as semiconductor fabrication itself, it was only a few years ago that our

understanding of the mechanisms of defect generation, pair diffusion and annealing has sufficiently matured to attempt predictive simulation. In Chapter 2 of this paper, I address the important issue of model calibration — the fitting of physically-based models to advanced experimental results.

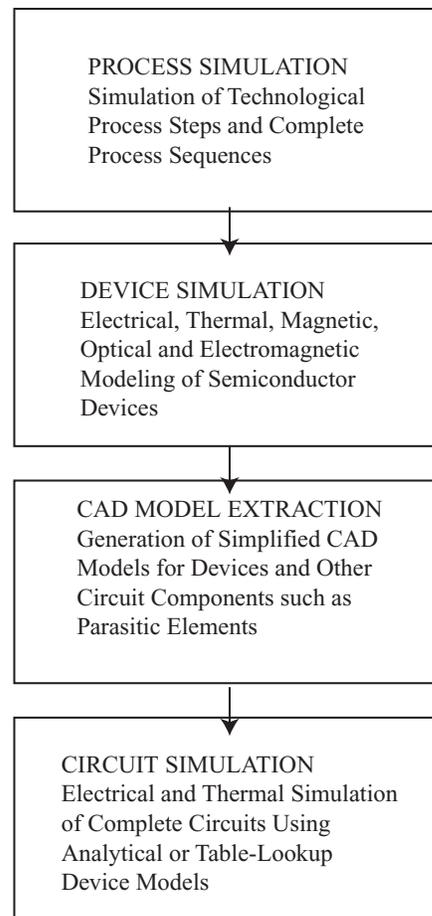


Fig. 1 The TCAD simulation hierarchy

Device simulation concerns itself with the physical modeling of current transport phenomena in semiconductor device structures. Depending on the application in mind and the device under study, electrical, magnetic, electro-magnetic and optical effects or possibly combinations

thereof can occur and need to be modeled. As can be expected, the range of models is wide, usually leading to coupled sets of nonlinear stationary or transient partial differential equations. In Chapter 3 of this paper, we provide different examples of applying TCAD to device analysis and optimization.

2 PROCESS SIMULATION AND MODEL CALIBRATION

In silicon microelectronics, the understanding of impurity diffusion is one of the oldest research topics awaiting a satisfactory solution. Over the past few years, considerable progress was made towards the goal of being able to accurately predict doping profiles. In today's advanced and extremely scaled MOS technologies, the formation of shallow junctions is of particular interest. While extremely challenging from a modeling viewpoint, the approach of calibrating the process models to advanced experiments such as secondary ion mass spectroscopy (SIMS) or nano-spreading resistance profiles seems to be quite successful. The following two figures are proof of the promising calibration methodology.

2.1 Ion implantation

The physical modeling of ion implantation is one of the most successful areas in TCAD. Both analytical as well as particle-based concepts have shown great promise in real applications. Figure 2 shows one example for low energy arsenic implants into silicon. Results such as this one can be routinely produced by professional TCAD software [1] for a wide range of operating conditions.

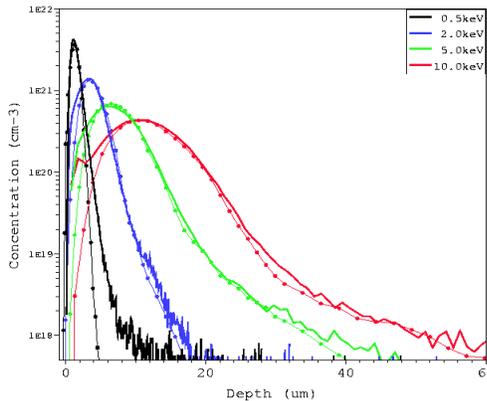


Figure 2. Comparison of experimental (SIMS) As profiles (dots) with modeling results obtained from a Monte-Carlo particle-based simulation [2].

2.2 Rapid thermal annealing

Compared to implantation, accurate and physics-based simulation of thermal annealing steps is considerably more challenging. Impurity diffusion in silicon occurs via a pair-diffusion mechanism: impurity atoms join one or more point defect (usually an interstitial). These point defects are generated during previous process steps such as an ion implantation. Modern technologies require very shallow junctions below 0.1 μm , which leads to rather short annealing times in the range of a few seconds. Therefore, the diffusion kinetics can be characterized as extremely nonlinear and non-stationary, putting stringent conditions on the numerical methods employed for equation solution. While many aspects of the impurity-defect clustering and declustering processes is still unknown, today's models show some promise that we are on the right track.

Figure 3 is a typical example of what can be achieved with mature and well calibrated TCAD tools.

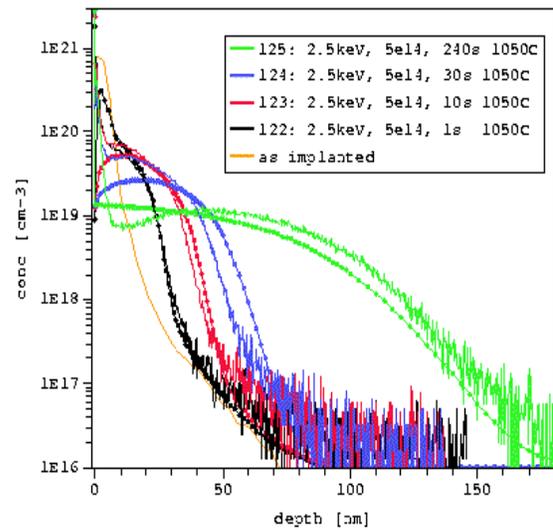


Figure 3: Rapid thermal annealing of an As implantation profiles for four different times. Dots designate SIMS results, and the (partly noisy) lines are from Monte-Carlo simulations. Results from [1].

3 DEVICE SIMULATION

As was already mentioned, device simulation spans a very wide range of applications. To illustrate the power and versatility of predictive device TCAD, I have chosen three representative examples :

1. simulation of parasitic bipolar devices in a smart power technology, and
2. Investigation of ESD protection elements in silicon VLSI.

3.1 Modeling of parasitic bipolar transistors in automotive applications

Control ICs for power management combine digital blocks and power stages (smart power) and work under extreme environmental conditions (automotive applications). When an inductive load, controlled by the smart power IC, is switched, the potential of a power stage n-well can dive below the substrate (p-type) potential. The switching periods to be considered are of the order of 10 μ s and above. Under these below-substrate conditions a considerable amount of electrons is injected into the substrate. Furthermore, holes can be injected through a parasitic PNP in the above supply conditions. These carriers significantly risk destroying the functionality of logic components. Carriers in the substrate may be collected by a CMOS well and can induce latch-up.

In order to investigate this issue, a three-dimensional full chip simulation must be performed. Figure 4 shows the simulated potential distribution on the chip under electron injection at the low side power stages.

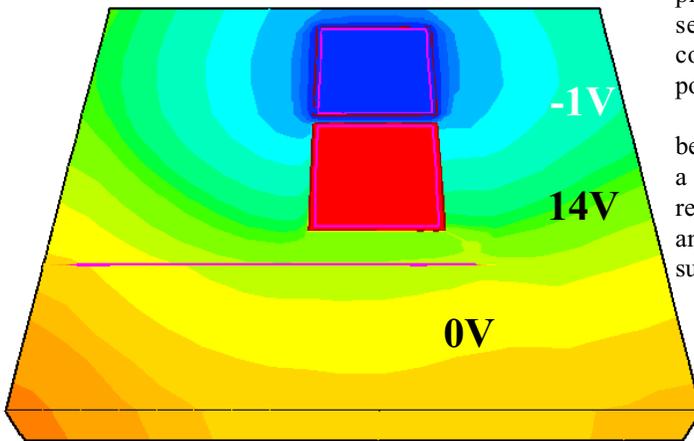


Fig. 4 Simulated distribution of the substrate potential on the test chip.

Figure 5 compares measurement and 3d-simulation of the parasitic NPN-transistor.

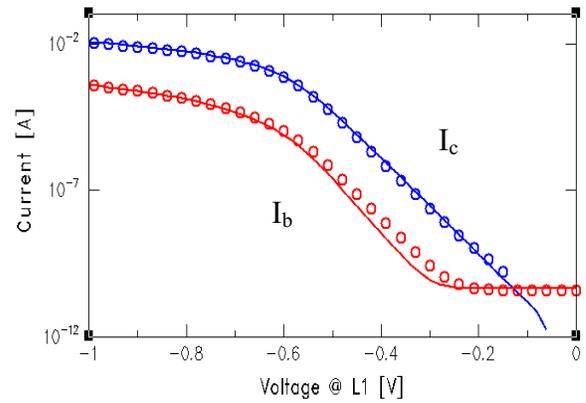


Fig. 5 Comparison of measurement (lines) and 3d-simulation (dots) for the collector and the base current of the parasitic NPN-transistor.

3.2 ESD Protection devices

The accurate prediction of the electro-thermal behavior of ESD protection devices belongs to the most challenging TCAD problems. Under conditions of ESD stress, a protection device typically is forced into first or even second breakdown conditions. For simulation, this corresponds to an extremely non-linear situation with possibly unsatisfactory convergence behavior.

While the characteristics of protection devices have been successfully modeled before, it was only recently that a complete comparison of experimental and simulated results was made for a wide range of operating conditions and device technologies [4]. The following two figures summarize the most salient points of this comparison.

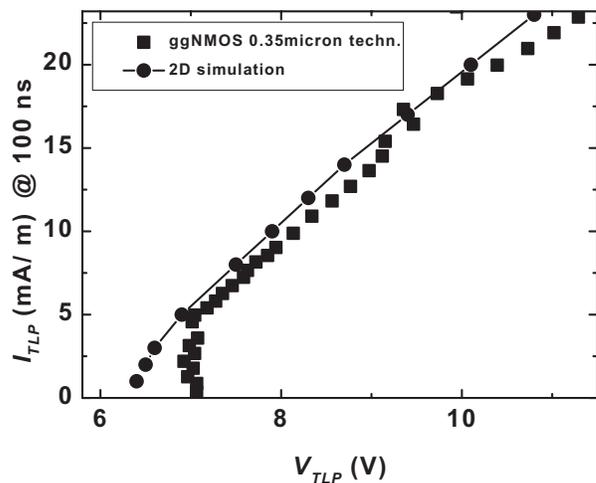


Fig. 6a

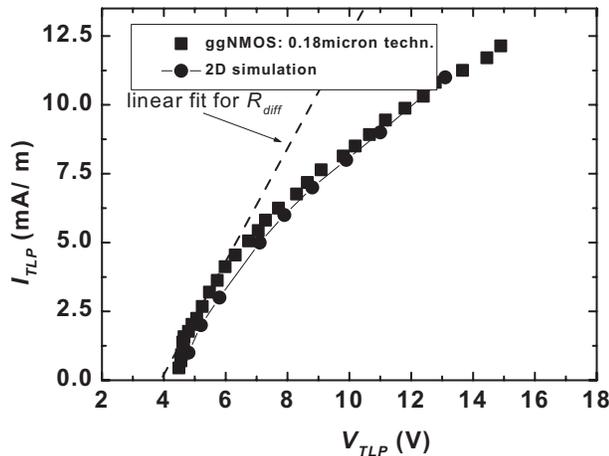


Fig 6b. Measured and 2D simulated high current IV characteristic for a reference grounded gate NMOS ESD device in the 0.35 (a) and 0.18micron (b) technology. The sustaining point of the 0.35^o technology is superimposed by 3D effects (inhomogeneous triggering), becoming apparent by the kink in the characteristic. The characteristics of the 0.18 transistor is strongly bent as result of internal heating.

4 FAB INTEGRATION AND TCAD FOR MANUFACTURING

The latest trend in TCAD applications is the full integration of software tools in a manufacturing environment (see Fig. 7, [5]). In a semiconductor factory, the flow of wafers between the various equipment stages is software-controlled through a manufacturing-execution-system (MES). This MES loads a flow for a particular process together with the required recipes from internal databases. Through standardized interfaces, it then sequences the process steps on the corresponding production equipment. Similarly, it controls the wafer measurements and collects statistical information for quality assurance.

The TCAD environment can very elegantly mirror the MES architecture in the fab by constructing a virtual environment. Once individual process steps have been calibrated to the equipment used, they can be efficiently and accurately utilized in the simulation of complete process flows.

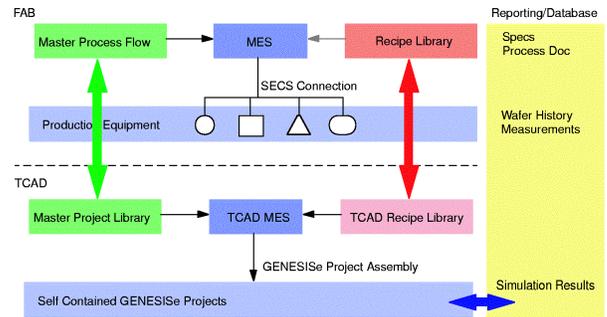


Fig. 7 TCAD tool integration in a fab environment.

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