Compact Modeling and Circuit Impact of a Novel Frequency Dependence of Capacitance in RF MOSFETs

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ABSTRACT

The exploration and modeling of high-frequency MOSFET phenomena are vitally important because MOSFETs are emerging as candidates for active devices in front-end RF circuits operating at more than 1GHz [1-2]. In this work we present a novel frequency-dependecnce of MOSFET capacitance, predicted in numerical device simulation and observed in measurements. Hitherto unobserved and unexplained, the phenomenon includes a drop in C_{BG} (and C_{GG}) with frequency in the accumulation regime, and changes in the weak-inversion regime. This behaviour is explained with the help of finite substrate resistance and non-quasi-static effects. Conventional quasi-static MOSFET compact models do not replicate the frequency dependence; a non-quasi-static MOSFET model developed in Motorola successfully models the frequency dependence of capacitance components. This model is used to demonstrate the impact of the novel frequency-dependence in simple RF-circuits.

Keywords: high-frequency, compact-model, MOSFET, RF, circuit, capacitance, inversion, accumulation.

1 INTRODUCTION

The growing importance of portable computing and hand-held communicators has caused low-power RF technology to be responsible for a larger and larger fraction of world-wide semiconductor sales. Reducing chip costs and power-consumption by migrating from traditional RF-BJT to RF-MOSFET technologies is an industry-wide trend [1-2]. An important obstacle is the lack of understanding of high-frequency phenomena in MOSFETs. Another equally important problem in designing RF MOSFET circuits in a mixed-signal or system-on-chip context is the inability of traditional (digital) MOSFET compact models to capture all the relevant high-frequency phenomena.

By convention, in this work "C_{AB}" is used to denote the capacitance with small-signal current measured at node *A* when a small-signal voltage is applied at node *B*. There is typically a DC voltage at node *B* that is swept (or stepped).

MOSFETs typically used in digital, analog and RF circuits are symmetric, such that the source and the drain can be interchanged with no change in electrical behaviour. In addition, asymmetrical MOSFETs such as Graded-Channel MOSFETs have also been used for digital and RF applications [3-4]. The high-frequency behaviour of MOSFET capacitances described in this work applies equally to symmetrical and asymmetrical MOSFETs; due to space limitations, only symmetric MOSFETs are discussed here. It must be noted that in a MOSFET when the small-signal voltage is applied to the gate electrode, charge conservation requires that $C_{GG} + C_{SG} + C_{DG} + C_{BG} = 0$. Here *G* refers to the gate, *S* to the source, *D* to the drain and *B* to the body (substrate). If only the magnitudes of the charges and capacitances are considered, it is easily shown that

$$|C_{GG}| = |C_{SG}| + |C_{DG}| + |C_{BG}| \quad (1)$$

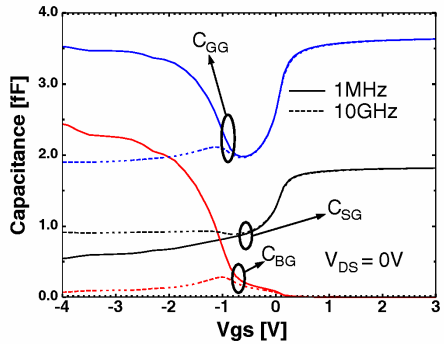

Fig. 1. $C(V_{GS})$ curves for an N-channel MOSFET at two frequencies, numerically simulated using MEDICI [6]. In the accumulation regime there is a drop in C_{BG}, a rise in C_{SG} (and C_{DG}) and an overall drop in C_{GG}, as frequency is increased. It is easily verified that Eq. 1 holds for both frequencies.

The novel frequency-dependence of capacitance which is studied in this work, has first been predicted in numerical device simulation and later observed in measurements of short-channel MOSFETs. Fig. 1 shows typical C-V curves for an n-MOSFET from numerical device simulation. At low frequencies, it is evident that in going from the accumulation regime ($V_{GS} << V_{TH}$) to the strong inversion regime ($V_{GS} >> V_{TH}$), C_{SG} (and C_{DG}) monotonically rise, while C_{BG} monotonically drops. As a result C_{GG} has the well-known minimum near V_{TH}. As frequency increases into the GHz range, the behaviour in the weak-inversion regime changes to a small extent. A more dramatic change is seen in the accumulation regime: as frequency increases, C_{BG} drops and C_{SG} (and C_{DG}) rises, and there is an overall drop in C_{GG}. This frequency-dependence of capacitance

components has not been reported before, and will be analyzed in this work.

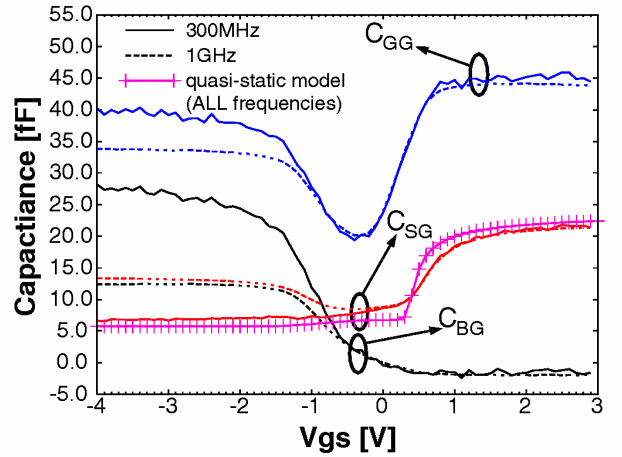

Fig. 2. Measured $C(V_{GS})$ curves for an N-channel MOSFET with $L_{poly}=0.5mm$, showing qualitative agreement with numerical simulations in Fig. 1. The quasi-static compact model shows no frequency-dependence, as shown by the C_{SG} simulation in SPICE. Note that for this particular device even a frequency as low as *300MHz* causes some high-frequency effects, which is why $C_{GG,accumulation} < C_{GG,inversion}$.

Fig. 2 shows measured C-V curves for an n-MOSFET and qualitative agreement with numerical simulations in Fig. 1. These C-V curves were obtained from S-parameter measurements using HP-equipment, followed by de-embedding of Y-parameters. Capacitance was then obtained using $Y_{AB}=G_{AB}+jwC_{AB}$, where G_{AB} is the conductance, $w=2pf$, and f is the frequency. In Fig. 2, negative values of C_{BG} are an artifact of the de-embedding scheme; in reality $C_{BG}=0$ for $V_{GS}>V_{TH}$.

In the following sections an explanation is provided for the high-frequency phenomenon, and its circuit impact is discussed.

2 PHYSICAL MODEL

The origin of low-frequency capacitance is well understood [7]. Hitherto unexplained, the decrease in C_{BG} with increasing frequency, shown in Fig.s 1-2, may be explained as follows: when the transistor is in the accumulation regime, the region below the gate oxide consists of a layer of holes whose density is higher than the background p-type doping. This hole-charge is supplied by the body contact, which is situated several microns (and in some cases several hundred microns) from the channel. When an oscillation in the gate voltage induces an oscillation in the accumulation charge, the speed with which these carriers can be supplied from the body contact is limited by the body-resistance (substrate resistance), which forms a series "RC" combination with the gate-oxide capacitance. As a result, the higher the frequency, the smaller is the response from the body contact, and the smaller is the body-gate capacitance (C_{BG}).

In the accumulation regime, the gate voltage has the combination of a large DC negative value and a small-signal perturbation. *S*, *D* and *B* contacts are grounded. During the positive cycle of the body current oscillation, holes are transported from the body contact to the accumulation region. The accumulation region thus acquires a small, negative voltage, which in turn causes the source-channel and drain-channel diodes to become slightly reverse biased. Additional holes can therefore be supplied to the accumulation region from the drain and source contacts, via reverse-bias currents in the diodes. In the negative cycle of the body-current oscillation, the *S-B* and *D-B* diodes become slightly forward-biased, due to the fact that a hole current passes through the substrate resistor and out of the substrate contact. Some of the holes can thus exit the device through the source and drain, via forward-bias currents in the diodes. In each half of the cycle, therefore, accumulation layer holes have three alternative paths to/from the ground terminal: a large-delay path to the body contact and relatively quick paths to the source- and drain-contacts. As a result, all three contacts contribute to the oscillation of the hole-charge. In the accumulation regime, the overall decrease in C_{GG} with increasing frequency is attributed to the fact that all three paths to ground involve increased delays, which prevents the device from fully supporting the accumulation-charge oscillation.

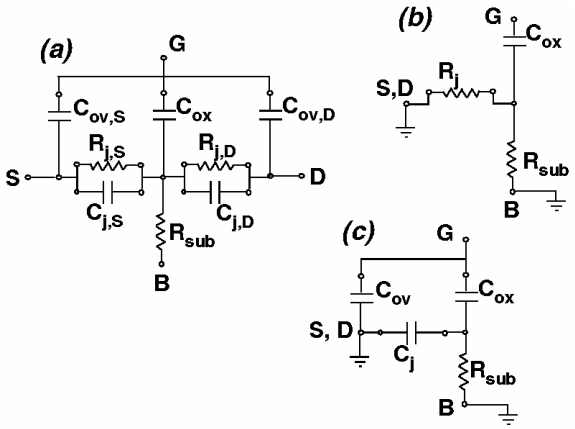

Fig. 3. Small-signal equivalent circuits for the MOSFET (a) in the accumulation regime, (b) in the low-frequency approximation, for $V_{DS}=0$ and (c) in the high-frequency approximation. C_{ov} is the *G-S* (*G-D*) overlap capacitance and C_j is the *S-B* (*D-B*) junction capacitance, and R_j the junction resistance. R_{sub} is the substrate (body) resistance.

Another way to understand these phenomena is to look at a small-signal linear equivalent-circuit model for the accumulation regime, in Fig. 3(a). The impedance between

the source and the accumulation region is modeled as the parallel combination of a resistor and a capacitor, to represent the zero-biased *S-B* diode. (A similar model is used for the *D-B* diode.) Clearly, as the frequency increases, the *S-B* diode impedance drops, and is dominated by the capacitance $C_{j,S}$, which explains the increase in small-signal source and drain currents, and consequently the increase in C_{SG} (and C_{DG}).

From Fig. 3 it is clear that $C_{ox} >> C_{ov}$, because C_{ov} is the sum of the gate-source ($C_{ov,S}$) and gate-drain ($C_{ov,D}$) fringe and overlap capacitances. Further, for typical MOSFETs it is observed that $C_{ox} > C_j$, where C_j is the sum of zero-bias capacitances for the *S-B* and *D-B* diodes. Furthermore, since R_j is the parallel combination of zero-bias resistances for the source-body ($R_{j,S}$) and drain-body ($R_{j,D}$) diodes, and since R_{sub} is the equivalent substrate resistance, it is easy to see that $R_j >> R_{sub}$.

These relationships allow us to conclude that at low frequencies, as described in Fig. 3(b), the input impedance looking in at the gate is simply a series combination of R_{sub} and C_{ox}; since the impedance magnitude of C_{ox} (that is, $1/wC_{ox}$) is large in comparison with R_{sub}, we can say that the input impedance is dominated by C_{ox}, the oxide capacitance. This means that C_{GG} should saturate to the C_{ox} value deep in accumulation. In fact measurements and numerical simulations show that this is indeed the case, as in Fig.s 1-2. At high-frequencies, the input impedance at the gate takes on a different form. As can be seen in Fig. 3(c), the impedance magnitude of C_j (that is, $1/wC_j$) is small, and at a sufficiently high frequency (typically in the GHz range), it dominates over the shunt-resistance, R_{sub}. The input-impedance can therefore be simplified into the parallel combination of C_{ov} and C, where C is the linear combination of C_{ox} and C_j. Since $C_{ox} > C_j$, $C \leq C_j$. This means that the input impedance at the gate is $\leq (C_{ov} + C_j)$, which we know can be considerably smaller than C_{ox}. This implies, therefore, that C_{GG} is smaller (in magnitude) in the high-frequency limit than at low frequencies. Once again, this is borne out by measurement and numerical simulations (Fig.s 1-2).

3 COMPACT MODELING

As shown in Fig. 2, conventional quasi-static models such as BSIM3 [5] do not display the desired frequency dependence of capacitance. Due to this reason, a multi-section non-quasi-static model has been developed [8]. The model represents the channel as a combination of multiple sections stretching from source to drain. The doping level and length of each section can be altered independently. Each section is modeled using a new physics-based compact model [9]. The penalty paid for the inclusion of *n*-sections is the computational burden posed by *n*-1 internal nodes, whose voltages have to be iteratively evaluated. In the interests of simulation speed, it is thus necessary to minimize the number of internal nodes.

The efficacy of the new model is demonstrated here. Fig.s 4(a) and (b) show that the new compact model replicates correctly the voltage- and frequency-dependence of various capacitance components. The only external element required for the model is a lumped substrate resistance, which is not present in the intrinsic multi-section non-quasistatic model. It is found that two channel sections are sufficient for describing the behaviour at various frequencies. The computational penalty for this model versus a single-section model is very circuit-dependent, and is about two-fold for a single-transistor simulation. The reader may note that the fits to measured C_{SG} in the near-threshold regime are not perfect. The discrepancy in this regime may be attributed to the drawbacks inherent in the empirical model for the voltage-dependence of C_{ov}, which exist in the older compact models and have been carried over to the new model. Inclusion of a physics-based voltage-dependence of C_{ov} will eliminate this problem.

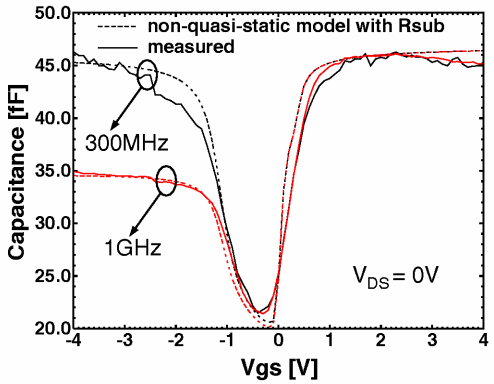

Fig. 4(a). C_{GG} from measurements and compact modeling for a fabricated N-channel MOSFET at two frequencies. The non-quasistatic compact model has two channel sections and an external R_{sub}. The MOSFET structure and doping in this case are slightly different from that in Fig. 2.

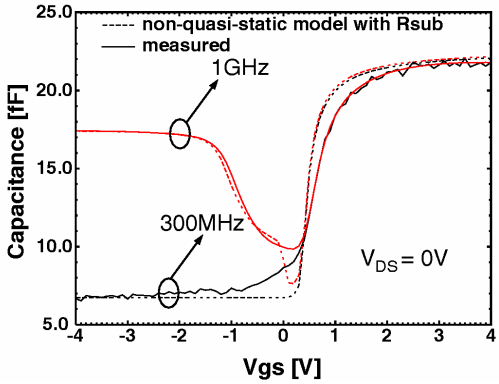

Fig. 4(b). C_{SG} from measurements and compact-modeling for an N-channel MOSFET at two frequencies, for the device in Fig. 4(a). The non-quasistatic compact model has two channel sections and an external R_{sub}.

To verify the qualitative model developed in the previous section, the source-body and drain-body diode models were omitted in the simulation, and it was found that this prevented accumulation regime C_{SG} from increasing with frequency. This supports the idea that the increase in C_{SG} is the result of the increasing admittance of the source-body diode with frequency. Additionally, it is clear from Fig. 3(a) that if R_{sub} is set to zero, capacitor C_j is shunted out, which means that the input circuit at the gate consists of C_{ox}, independent of frequency. Sure enough, when R_{sub} was omitted from the compact model, it was observed that C_{GG} saturated in the accumulation regime to C_{ox} for all frequencies.

It has been shown that a compact model exists for the accurate representation of the novel high-frequency MOSFET phenomenon. The next step is to study the impact of these newly discovered frequency-effects on the performance of the device in a circuit.

4 CIRCUIT IMPACT

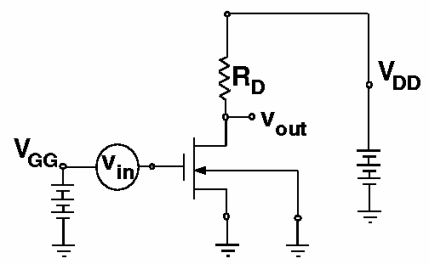

Fig. 5. Schematic for a simplistic RF common-source amplifier simulated in SPICE using a multi-section, non-quasistatic model. Here $V_{DD}=3.5V$, $V_{GG}=1.8V$, $V_S=V_B=0V$ and $R_D=2kW$.

The new compact circuit model is applied to a simple RF circuit, namely a simple common-source, N-channel MOSFET amplifier. The device chosen for this study has $L_{poly}=1.6mm$ and $W=21mm$. Prior to simulating the circuit, the DC characteristics of this device were matched to measurements by fine-tuning various parameters in the single-section model. Following this, the single section channel was converted into a *three-section* channel, where each section had a length of 0.4μm.

The circuit (see Fig. 5) has $V_{DD}=3.5V$, $V_{GG}=1.8V$ and $V_S=V_B=0V$. The bias/load resistor, R_D is 2kΩ. In order to model the accumulation regime frequency dependence explained in section 4, a substrate-resistor is necessary. However, since the device operates entirely in the strong-inversion regime ($V_{GS} > V_{TH}$), the omission of R_{sub} does not significantly change results.

It is seen that in the presence of a drain resistor and unequal drain and source biases ($V_{DS} > 0$), the impact of multiple channel sections is significant. As Fig. 6 shows, the inclusion of the multiple channel-sections considerably alters the small-signal gain behaviour as a function of frequency. It may be argued that a drop in gain arising from the inclusion of additional passive parasitics can be easily "matched-out" by a suitable matching network. However, without a suitable compact model, such as the one described in this work, accurate designs are not possible. In the circuit considered here, it is the ON-state capacitance behaviour that plays an important role and requires correct modeling. It is possible that OFF-state (accumulation regime) effects are also important in other circuits.

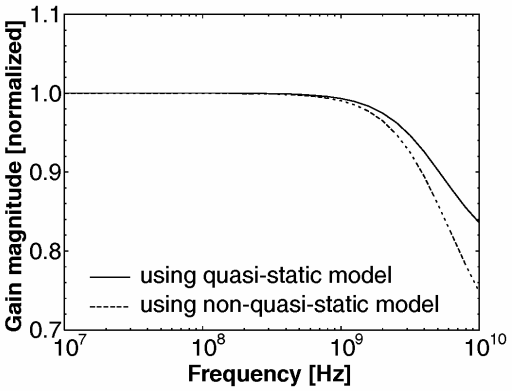

Fig. 6. Small-signal gain magnitude (defined as the magnitude of v_{out}/v_{in}) for the amplifier in Fig. 5. The new compact model improves the estimation of various parasitics and indicates a drop in the gain magnitude.

5 CONCLUSIONS

A novel frequency dependence in MOSFETs has been identified and explained. It has been modeled for circuit simulation using a multi-section, non-quasistatic representation, along with a substrate resistor. The impact of the novel phenomenon on ON-state circuit performance of the MOSFET has been quantitatively studied. The importance of this work is underscored by the industry's move towards the use of MOSFETs for RF front-ends in portable products.

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