Substrate Current Simulations at Elevated Temperatures

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ABSTRACT

We report results of hydrodynamic simulations and measurements of substrate currents in submicron MOSFET. Both simulations and measurements show anomalous dependence of the substrate current on lattice temperature, which is consistent with previously published experimental results [1]. This unusual behavior of substrate current is due to the dependence of the electron energy relaxation length on lattice temperature, and cannot be explained within the commonly used drift-diffusion transport model.

Keywords: MOS, substrate current, hydrodynamics, simulation.

1 INTRODUCTION

Substrate current is traditionally used for monitoring hot-carrier induced degradation. Therefore, it is very important that device simulators predict, with reasonable accuracy, substrate currents for advanced MOS devices in the wide range of applied biases, temperature conditions, etc. The drift-diffusion approach, combined with a local-field model for impact ionization, is widely used in the industry for MOS simulations. Unfortunately, this relatively simple and efficient model has very restrictive capabilities for substrate current simulations because it treats the ionization rate as a function of the local electric field rather than the carrier energy.

Novel experimental results evaluating substrate current dependence on lattice temperature have been published in [1]. Substrate current in submicron transistors for low drain voltages is found to increase at higher temperatures, contrary to the trend observed for long channel devices. This anomalous behavior cannot be explained within the drift-diffusion approach because there is no mechanism in the field-dependent impact ionization model to enhance the ionization (substrate current) at elevated temperatures. The Monte Carlo simulations indicate [2] that highly temperature sensitive tail of electron energy distribution is responsible for this anomalous behavior.

In this report, we demonstrate that the same physical phenomenon can be also described on hydrodynamic rather than microscopic (kinetic) level. We compare substrate current simulations, using hydrodynamic approach and energy dependent impact ionization model to measurements at different temperatures. This comparison shows that our simulation approach and physical models correctly predict anomalous temperature dependence of substrate current in submicron devices. The physical mechanism responsible for this anomalous behavior is discussed.

2 RESULTS AND DISCUSSION

The general purpose device simulator, DESSIS [3], was used for the simulations. A hydrodynamic transport model with the energy dependent impact ionization rate based on Chynoweth formulas, with coefficients from [4], was used.

The structure studied in this paper was a quarter micron NMOS transistor with double diffused source and drain. Figure 1 shows simulated and measured substrate currents versus gate voltage for two drain biases and two lattice temperatures.

The simulation quality is evident in the excellent agreement with measurements, which is even more remarkable considering that no special calibration was performed. Both simulated and measured results indicate that the maximum substrate current increases for higher lattice temperatures, which is contrary to the previously observed behavior in long channel devices. The simulations capture the values of the maximum substrate current and the gate voltages at which this maximum is reached. For Vd=1.6V and gate voltages higher than 1V, the simulated curves have steeper falling slopes than the experimental data. We think that this minor discrepancy is due to constant (energy independent) energy relaxation time used in our simulations.

Figure 2 displays the simulated and measured drain current as a function of gate voltage for the same conditions. The drain current shows conventional behavior (see Figure 2) in that it decreases with increasing temperature, which is consistent with mobility degradation at higher temperatures.

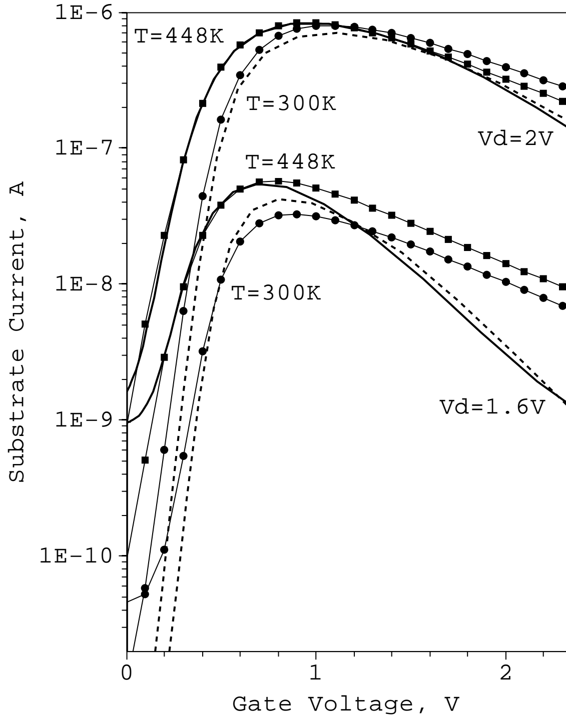

FIGURE 1. Substrate current versus gate voltage. Vd=1.6V and 2V. T=300K (circles and dashed curves) and 448K (squares and solid curves). Curves with markers represent the measurements.

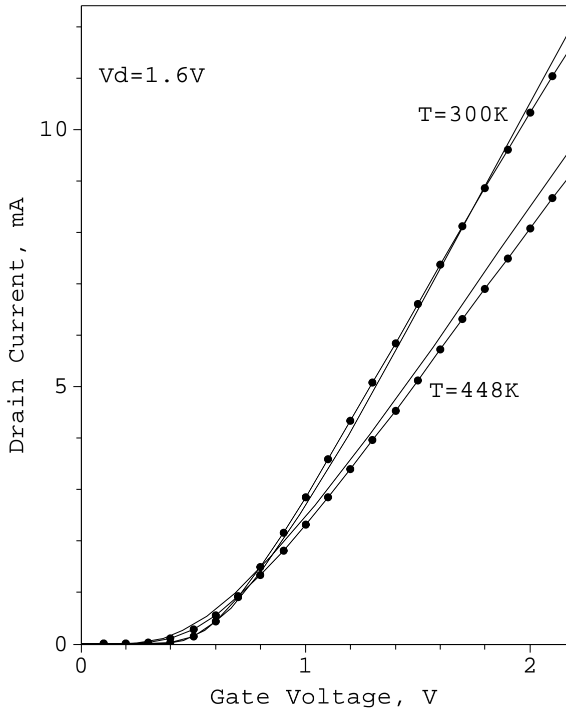

FIGURE 2. Drain current versus gate voltage. Vd=1.6V. T=300K and 448K. Curves with markers represent the experimental results.

It was observed in [1] that the anomalous temperature behavior of the substrate current turns back to normal at higher drain biases. The drain bias at which this transition back to normal behavior happens is called the crossover voltage. For our device the experimental crossover voltage slightly exceeds 3V on the drain. Our simulations do not show the crossover at Vd=3V but show it at Vd=4V (see Figure 3). It must be noted that the crossover voltage is very sensitive to the doping concentrations and lattice temperatures [1].

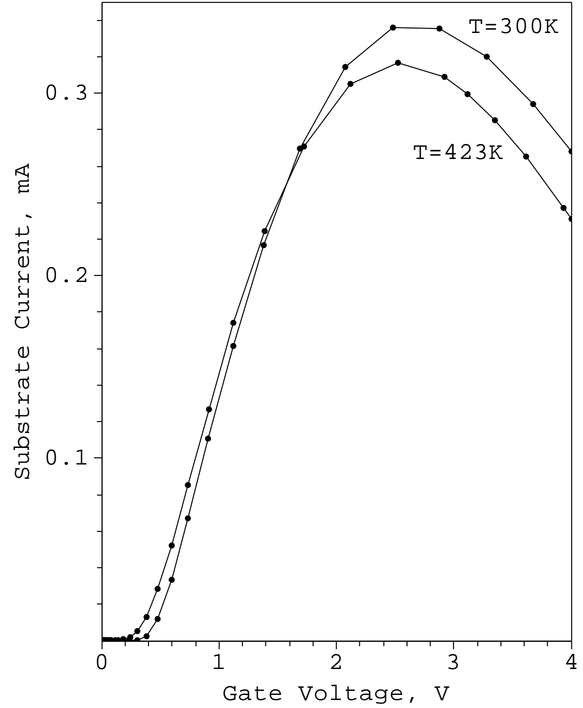

FIGURE 3. Substrate current as a function of gate voltage for Vd=4V. T=300K and 448K.

The model of impact ionization rate used in the simulations reads (for simplicity we consider just the electron part; for holes similar formulas hold):

$$G_n=\alpha\,|J_n|/q,\ \ \alpha=A\exp(-B\,\gamma/E_{eff}), \quad (1)$$

where J_n is the electron current density, A and B are constants determined for room temperature [4], E_{eff} is the effective electric field, and dimensionless factor γ takes into account the temperature dependence of the electron mean free path due to electron-phonon scattering and can be expressed as [5]:

$$\gamma=\tanh(\hbar\omega/2kT_0)/\tanh(\hbar\omega/2kT), \quad (2)$$

Here $\hbar\omega$ denotes the optical phonon energy, T_0=300K, and T is the actual lattice temperature.

In the framework of drift-diffusion models, E_{eff} is the component of electric field parallel to the current ($E_{||}$). At first glance, Eq. (1) suggests that G_n should decrease with increasing lattice temperature, resulting in a decrease in substrate current. This behavior is true for the drift-diffusion model. Indeed, J_n decreases (mobility degradation), γ increases, and $E_{||}$ is almost independent of temperature. The situation changes dramatically if one uses hydrodynamic model. In this case the effective electric field is given by

$$E_{eff} = 3/2\, k\, (T_n - T)/q\, \lambda, \tag{3}$$

where T_n is the electron temperature, λ is the energy relaxation length, $\lambda = v_s\, \tau_w$, with v_s being the saturation velocity and τ_w the energy relaxation time.

Expression (3), which determines the relationship between E_{eff} and electron temperature T_n, can be derived from the energy balance equation under uniform conditions where the energy gain in electric field is equal to the energy loss due to scattering. Expression (3) is widely used in the framework of hydrodynamic transport model. As long as v_s, and therefore λ, significantly decreases with increasing lattice temperature, E_{eff} can increase (and really does) at higher lattice temperatures despite decreasing of T_n. This effect can dominate over the other factors which work to diminish the impact ionization rate. Hence, it can cause an increase of the impact ionization rate and ultimately the substrate current.

For qualitative understanding of the dependence of effective field on lattice temperature (energy relaxation length), let us consider a simple analytical relationship between E_{eff} and $E_{||}$ [6]:

$$E_{eff}(x) = 3/5\lambda \int_0^x dy\; E_{||}(y)\, \exp[-3(x-y)/5\lambda)], \tag{4}$$

The integration in Eq. (4) is done along the channel from source to drain, and the electron temperature at x=0 is equal to the lattice temperature. Let us simplify Eq. (4) by assuming that $E_{||}$=const. Then we obtain:

$$E_{eff}(x) = E_{||}\, [1 - \exp(-3x/5\lambda)], \tag{5}$$

It follows from expression (5) that E_{eff} is always less than $E_{||}$ (a well known fact), and that E_{eff} increases if λ decreases. Consequently, we again see that E_{eff} increases at higher temperatures since λ decreases.

Figure 4 shows the effective electric field (E_{eff}) distribution along the channel at two lattice temperatures obtained from 2D numerical simulations of the above MOSFET.

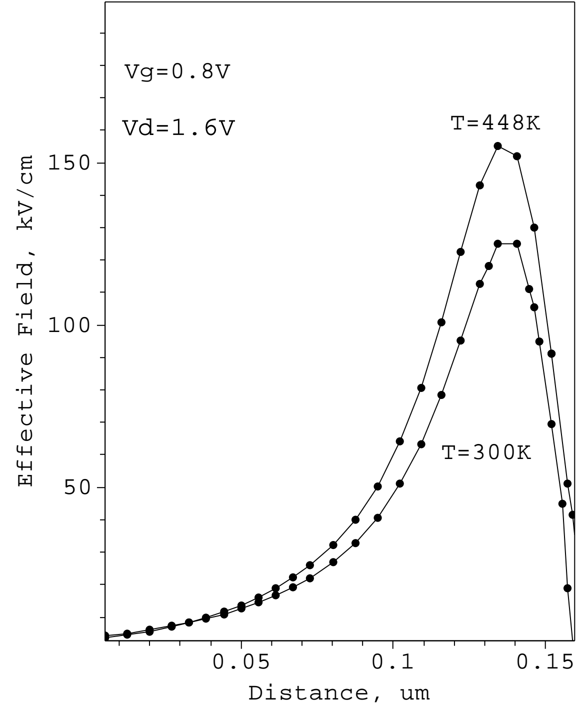

FIGURE 4. Effective field distribution along the channel. Vg=0.8V, Vd=1.6V. T=300K and 448K.

A dramatic increase of the effective field at T=448K is observed, despite the fact that electron temperature peak is higher at 300K (see Figure 5). This explains the increase of the substrate current at T=448K compared to T=300K and proves that the decrease of the energy relaxation length at elevated temperatures is responsible for this anomalous behavior.

It must be noted that in older technologies with longer channel devices and much smoother doping profiles, non-local effects are substantially less pronounced. Therefore, a slight increase in E_{eff} cannot compensate for the other factors which diminish the impact ionization rate. This is the reason why the “usual” decrease of the substrate current at elevated temperatures has frequently been observed both experimentally and in prior simulations.

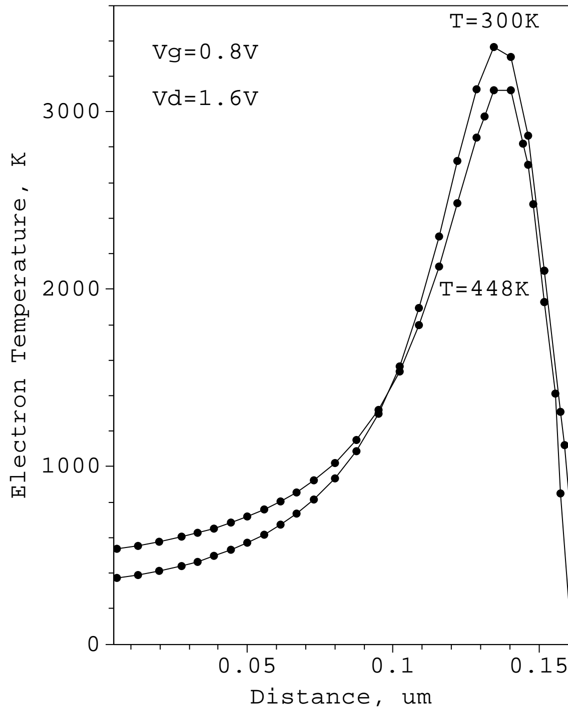

FIGURE 5. Electron temperature distribution along the channel. Vg=0.8V, Vd=1.6V. T=300K and 448K.

3 CONCLUSIONS

A hydrodynamic approach with carrier energy dependent impact ionization rates has been used to simulate substrate currents in quarter micron MOS transistor. The simulations successfully predict the anomalous temperature dependence of the substrate current, in excellent agreement with experimental data. The decrease in energy relaxation length at higher temperatures is responsible for the increase of substrate current. We observe the increase of the effective field and impact ionization rates despite the decrease of the mean electron energy (temperature) at elevated lattice temperatures.

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