An Effective Potential Method for Including Quantum Effects Into the Simulation of Ultra-Short and Ultra-Narrow Channel MOSFETs

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ABSTRACT

Quantum effects are known to occur in the channel region of MOSFET devices, in which the carriers are confined in a triangular potential well at the semiconductor-oxide interface. Typically, these effects are quantified by a simultaneous solution of the Schrödinger and Poisson equations, which can be a very time consuming procedure if it needs to be incorporated in realistic device simulations. We have developed a simple and very efficient approach of approximating quantum effects by using an *effective* potential that takes into account the natural non-zero size of an electron wave packet in the quantized system. The benefits of the effective potential approach are that it eliminates the need for a full solution to the Schrödinger equation, thus leading to low additional computational cost. In this paper, the approach is applied in the investigation of the role of quantum-mechanical space-quantization effects in the operation of 0.1 μm MOSFET device and recently proposed SOI device structure.

Keywords: ultra-small MOSFETs, quantization, Monte Carlo simulation, SOI devices.

1. INTRODUCTION

Quantum effects are known to occur in the channel of MOSFETs, where the confinement is in the direction normal to the semiconductor/oxide interface. For quite some time, there have been attempts to determine the role this quantization plays in semiconductor devices. Often, this is found by coupled solutions of the Schrödinger and Poisson equations to find the actual position of the charge and the changes in mobility and capacitance [1,2]. This, however, can be a very time consuming procedure. For this purpose, we have developed a simple and very efficient approach of approximating quantum effects by using an *effective* potential that takes into account the natural non-zero size of an electron wave packet in the quantized system. This effective potential is related to the self-consistent Hartree potential, obtained from Poisson's equation, through an integral smoothing relation

$$V_{eff}(\mathbf{x}) = \int V(\mathbf{x}+\mathbf{y})G(\mathbf{y},a_0)d\mathbf{y}\,, \qquad (1)$$

where G is a Gaussian with standard deviation a_0. This method eliminates the need for a full solution of the 1D or 2D Schrödinger equation and has a low computational cost, with less than 10% increase in CPU time.

One of the questions that one would naturally ask when using this approach is related to the actual value of the Gaussian smoothing parameter a_0. Also, there has been a debate as to whether the smoothing parameter will depend upon the shape of the confining potential or the substrate doping density. For this purpose, we first apply the effective potential approach to simple MOS capacitor structure in which the band-bending leads to triangular confinement. The oxide thickness of the MOS capacitors being simulated is 6 nm, and the substrate doping equals 10^{17} and 10^{18} cm^{-3}, respectively. The results of these simulations are shown in Figures 1(a) and 1(b), where we plot the gate-voltage dependence of the inversion charge density, and the average distance of the carriers from the interface.

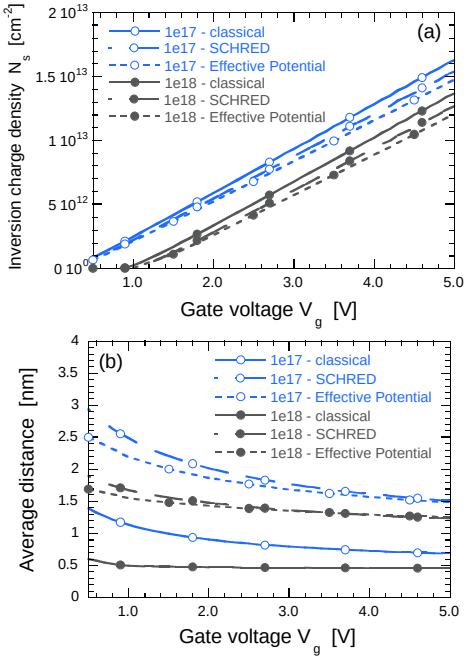

Fig. 1 (a) Sheet electron density and (b) average displacement of the carriers from the semiconductor/oxide interface, as a function of the gate voltage. For each doping density, we use classical charge description, fully quantum-mechanical charge description via SCHRED [3], and Gaussian smoothing of the Hartree potential (effective potential approach).

From the results shown in Fig. 1, it is obvious that the use of a single Gaussian smoothing parameter a_0 = 0.5 nm along the growth direction, can quite accurately describe the reduction in the inversion layer electron density due to quantum-mechanical space-quantization effect. It also leads to accurate description of the displacement of the carriers away from the semiconductor-oxide interface, which, in turn, gives rise to finite quantum capacitance, in series with the oxide capacitance.

The above described effective potential approach was introduced into three-dimensional MOSFET simulations in which the transport is handled by an ensemble Monte Carlo approach using non-parabolic bands and simulating particles (~30,000 typically) throughout the device rather than just in the channel. We consider two situations. The first is the case of a 50 nm MOSFET device, in which the major quantum confinement occurs in the direction normal to the oxide interface. In this case, we find that the threshold voltage is shifted and the carrier density is moved away from the interface, in excellent agreement with earlier simulations using a full solution to the Schrödinger equation. Importantly, the mean velocity of the carriers is not affected significantly by the introduction of this effective potential, and is only reduced by about 10%. Secondly, we consider a SOI MOSFET with a very narrow channel, such that quantum confinement is now two-dimensional and occurs both perpendicular and parallel to the oxide interface [4]. We find that a Gaussian smoothing parameter a_0 = 0.64 nm (the theoretical value) gives accurate charge description in the channel region of this device.

2. RESULTS FOR THE 50 nm MOSFET

A schematic of the 50 nm MOSFET we simulate is shown in Fig. 2. The channel doping equals 10^{18} cm^{-3}, source/drain doping is 10^{19} cm^{-3} and junction depth is 36 nm. The oxide thickness is 2 nm and the width of the device being simulated is 0.8 μm.

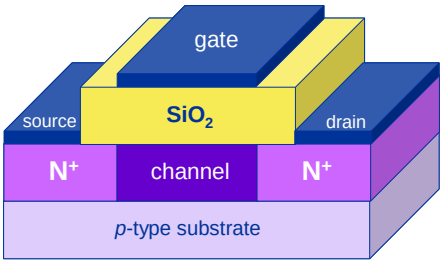

Fig. 2 Schematic of the 50nm MOSFET that is modeled

The 2D Poisson's equation is solved using an ILU decomposition method. A non-uniform tensor-product grid is used with 0.5 nm size normal to the interface and 1 nm parallel to the interface in the active channel region. In the actual simulation, ~30,000 particles are included, although most of the particles reside in the source and drain regions. In agreement with the earlier discussion, the values of the Gaussian smoothing parameter a_0 are taken to be 0.5 nm normal to the interface and 1.0 nm along the channel.

In Fig. 3, we show the conduction band edge, found in the device simulation, for the bias conditions V_G = V_D = 1V. From the results shown in the bottom panels, one can see that the effective potential shifts the conduction band edge upwards. It, thus, accounts for the so-called band-gap widening effect due to the quantum mechanical quantization in the triangular potential well near the Si-SiO_2 interface. The upward shift of the conduction band edge leads to a reduction of the carrier density at the interface proper. Also, the electron density is moved away from the interface because of the perpendicular field in the vicinity of the Si-SiO_2 interface. This later observation is more clearly seen in the results shown in Fig. 4, where we plot the average displacement of the electrons for two different bias conditions.

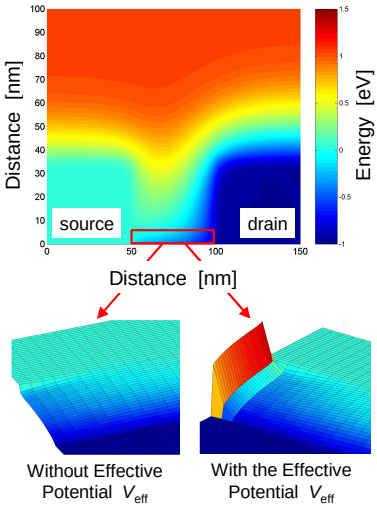

Fig. 3 Conduction band edge (top panel) for applied bias V_G = V_D = 1V. In the lower right (left) panel we plot the conduction band edge near the Si/SiO_2 interface when the effective potential is included (omitted) in the simulations.

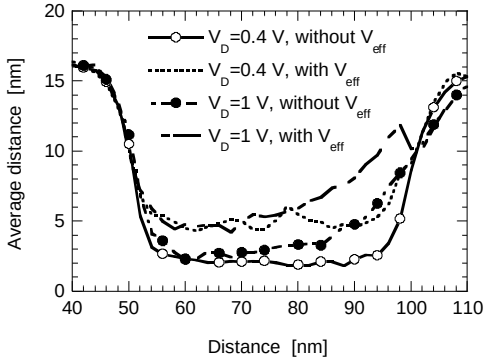

Fig. 4 The "center of charge" for the inversion electrons along the channel.

The quantization of charge in the inversion layer produces an expected increase of the threshold voltage in the channel. In Fig. 5, we plot the linear drain current as a function of the gate voltage, for a drain voltage of 0.1 V. It is clear that the turn-on of current is shifted by about 80 mV. The actual threshold voltage is quite difficult to determine in a Monte Carlo simulation. Here, we average the charge over the entire channel in order to estimate the inversion charge at any one point. This is done with low drain bias to keep the channel as homogeneous as possible.

In Fig. 6, we plot the device output characteristics. The observed reduction in output current is largely due to the increase in the threshold voltage in the device. Consequently, the quantization mainly affects this threshold voltage, which is a property of the confinement *normal* to the interface, whereas the transport is largely parallel to the interface. Also, the degradation of the drain current is larger for higher gate voltages, i.e. when the quantum-mechanical space-quantization effect at the source side of the channel becomes more prominent.

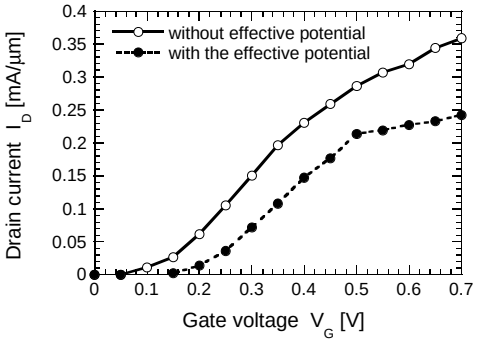

Fig. 5 Transfer characteristics of the 0.1 μm MOSFET device being simulated, in which one clearly sees the shift in the threshold voltage due to the quantum-mechanical space-quantization effect.

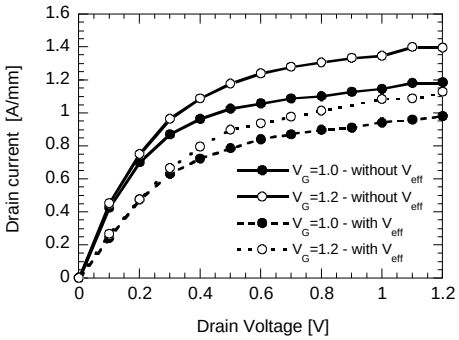

Fig. 6 The output characteristics for the device simulation discussed here. The decrease in output current, with the effective potential, is largely due to the threshold voltage increase.

3. RESULTS FOR THE SOI-DEVICE

A schematic of the SOI device structure [4] that we simulate is shown in Fig. 7 . It consists of a thick silicon substrate, on top of which is grown 400 nm of buried oxide. The thickness of the silicon-on-insulator (SOI) layer is 7 nm, with p^- region width between 7 and 15 nm. On top of the SOI layer sits gate-oxide layer, the thickness of which is 34 nm. The conductance of the channel is modulated with the variation of the top gate voltage. It is important to note that, in contrast to standard MOSFET devices, in which space quantization occurs along the depth of the device, the SOI device is an example of a device structure in which two-dimensional quantization effect (along the depth, or *y*-axis, and width, or *z*-axis) is important. This, in turn, necessitates the solution of the 2D Schrödinger equation if accurate charge description in the channel region of the device is desired. The repeated solution of the 2D Schrödinger equation at several slices perpendicular to the *x*-axis (device length), self-consistently with the 3D Poisson equation, can be very time-consuming process. For this purpose, as already mentioned earlier, we examine the applicability of the effective potential approach for this type of confining potentials.

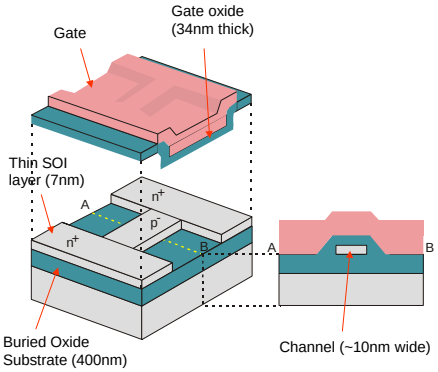

Fig. 7 Schematic description of the SOI device being investigated.

As for the case of a triangular confinement, we need to determine whether the theoretical model from Ref. [5] leads to appropriate Gaussian smoothing parameters along the depth and width of the device. To accomplish this task, we only consider the channel region of the device from Fig. 7, which, if uniform, is nothing more than a quantum wire, i.e. a structure in which carriers are free to move only along the *x*-axis, but are confined along the *y*- and *z*-axis. The simulation results for the electron line density obtained with the effective potential approach are compared against the self-consistent simulation results obtained via the solution of the 2D Schrödinger equation coupled with the 3D Poisson equation. We would like to point out that, because of the pronounced mass anisotropy in the Si material system and the multi-valley nature of the lowest conduction bands, the six conduction band valleys in Si are included through a standard three-valley model. Valley pair 1 points along the (100) direction having $m_x = m_l = 0.91m_0$ and $m_y = m_z = m_t = 0.19m_0$. Valley pair 2 points towards the (010) direction and has $m_x = m_z = m_t$ and $m_y = m_l$, and valley pair 3 points in the (001) direction, having $m_x = m_y = m_t$ and $m_z = m_l$. As a result of the above,

at each iteration step, one needs to solve the 2D Schrödinger equation, of the form

$$\left[-\frac{\hbar^2}{2m_y^{\nu}}\frac{\partial^2}{\partial y^2}-\frac{\hbar^2}{2m_z^{\nu}}\frac{\partial^2}{\partial z^2}+V(x,y,z)\right]\psi_j^{\nu}(x,y,z)=E_j^{\nu}(x)\psi_j^{\nu}(x,y,z), \quad (2)$$

three times, i.e. for each equivalent valley pair ν. Once the energy eigenstates and the corresponding eigenfunctions are known, the 3D electron density is found by using

$$n(x,y,z)=2\sum_{\nu=1}^{3}\sum_{j}N_j^{\nu}(x)\left|\psi_j^{\nu}(x,y,z)\right|^2, \quad (3)$$

where the factor of 2 accounts for valley degeneracy, the double sum represents summation over all energy eigenstates (index *j*) belonging to each of the three valley pairs (index ν) and the line charge density is given by

$$N_j^{\nu}(x)=\frac{1}{\pi\hbar}\sqrt{2m_x^{\nu}k_BT}\cdot F_{-1/2}\left(\frac{E_F-E_j^{\nu}(x)}{k_BT}\right), \quad (4)$$

where T is the temperature and k_B is the Boltzmann constant. In the actual evaluation of the Fermi-Dirac integral of order -1/2, which appears in Eq. (4), we use the following approximate expression [6]

$$F_{-1/2}(\eta)=\int_0^{\infty}\frac{u^{-1/2}du}{1+\exp(u-\eta)} \approx \frac{\sqrt{\pi}}{e^{-\eta}+\sqrt{\frac{\pi}{2}}\dfrac{1}{\sqrt{\eta+b+\left[a+\left(|\eta-b|\right)^c\right]^{1/c}}}}, \quad (5)$$

where $\eta=\left(E_F-E_j^{\nu}\right)/k_BT$, a=6.68, b=1.72 and c=4.11. The calculated gate-voltage dependence of the line density, for the test device structure with homogeneous confinement along the *x*-axis, is shown in Fig. 8. For each wire width (7, 10 and 15 nm) we use both the effective potential approach and the self-consistent solution of the 2D Schrödinger-3D Poisson problem. Excellent agreement is observed between the two approaches when using the theoretical value for the Gaussian smoothing parameter, which suggests that the effective potential approach can be used successfully for more complicated confining potentials. The transport properties of this device structure are currently being examined and will be presented elsewhere.

4. CONCLUSIONS

We used an effective potential approach to take into account the quantum-mechanical space-quantization effects in a 50 nm MOSFET device and SOI device structure. We find that the charge reduction and its average displacement from the interface lead to ~80 mV threshold voltage shift in the regular MOSFET device. This, in turn, gives rise to about 20% reduction of the on-state current. We also demonstrate that the effective potential approach can be successfully used in the case of more complicated confining potentials, such as the 2D confinement in the channel region of the SOI device from Fig. 7.

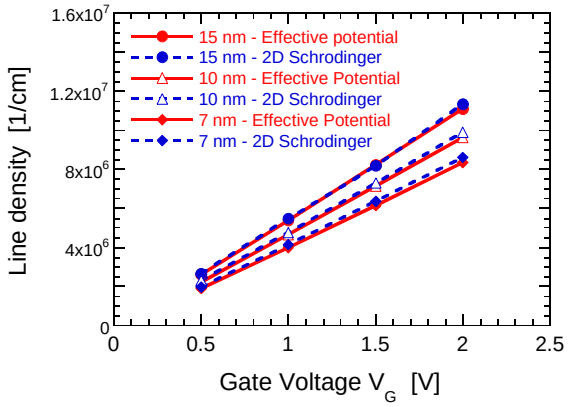

Fig. 8 Variation of the line charge density for a quantum wire that represents the channel region of the SOI device structure from Fig. 7. The wire width equals 7, 10 and 15 nm.

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