Mobility Degradation and Current Loss due to Vertical Electric Field in Channel Area of Submicron MOS Devices

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ABSTRACT

In this work we show quantified modeling results for the effect of gate-voltage-induced mobility degradation on MOS device current. Presented results are for three technologies, i.e. 0.50 μm, 0.35μm, and 0.25μm, and are based on extractions from measured data. Quantified results show that the calculated current loss due to this type of mobility degradation is increased with technology scaling and is reduced at higher temperatures. Measured values of the access resistance of the MOS devices for the three technologies as a function of temperature are also presented.

Keywords: Mobility degradation, MOS current drive, MOS current degradation.

1 INTRODUCTION

In deep submicron technologies with gate oxide thinness values of a few nano-meters, mobility degradation due to the vertical field in channel area is a major source of current loss. Obviously the field is generated by the gate bias. While vertical scaling provides undoubted advantages, current loss is an inevitable penalty due to this physical device effect. It is desirable to know exactly how much current will be lost due to this type of mobility degradation when the oxide is shrunk. It is not easy to measure and quantify this current loss. The purpose of this work is to answer this question quantitatively.

2 THE MODEL

The approach is to utilize an accurate physical MOS model that has proper tools for mobility degradation effects and to utilize the model for the calculation of the current loss due this mobility degradation. Selection of the model, accurate extraction of the parameter values, and to ensure the physical meaningfulness of each parameter is essential for this investigation. If physicality of the parameter values is lost, the final conclusions will not be accurate. Of special importance are the source/drain MOS access resistances, shown in Figure 1, because their effects on device characteristics is similar to those of

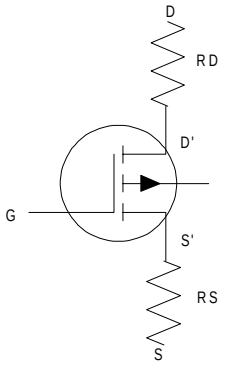

Figure 1. MOS device with S/D resistances

mobility degradation. So, for this investigation, accurate measurement of the MOS resistances is very important, independent of the selected MOS model. It was decided to use Philips MOS MM9 model for the core of the MOS device and to include the access resistances externally [1]. MM9 has proved strong and accurate in deep sub-micron devices, and covers the mobility degradation effects with details including geometrical and temperature dependencies.

3 DATA COLLECTION AND PARAMETER EXTRACTION

For data collection, wafers were selected from the line of production for 0.50μ, 0.35μ, and 0.25μ technologies. Comprehensive data was collected on a matrix of MOS devices with a variety of geometries for each technology [2], in a temperature range of 25 to 125C. Source/drain resistances were measured separately on the same temperatures [3]. Measured values of Rs and Rd are shown in Figures 2 and 3. For each technology at each temperature, the correct value of the Source/drain resistance was used in the circuit of Figure 1. MM9 model parameters were then extracted using the internally developed procedure in central R&D Crolles, France [2].

4 RESULTS & DISCUSSION

Results in Figures 2 and 3 show that for the three technologies, the value of the access resistance is reduced with device scaling with some increase by temperature.

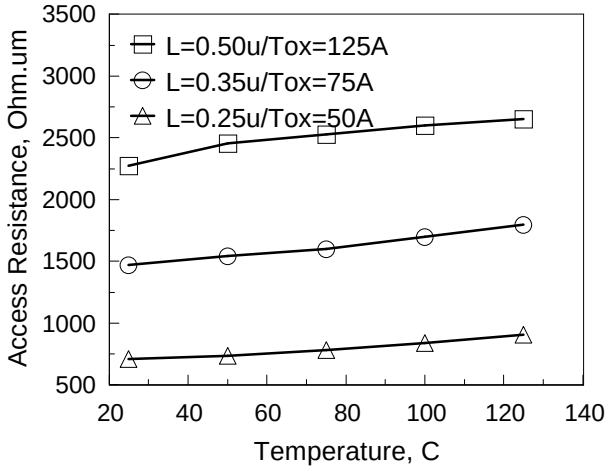

Figure 2. Measured access resistance values for Pchannel devices for three technologies.

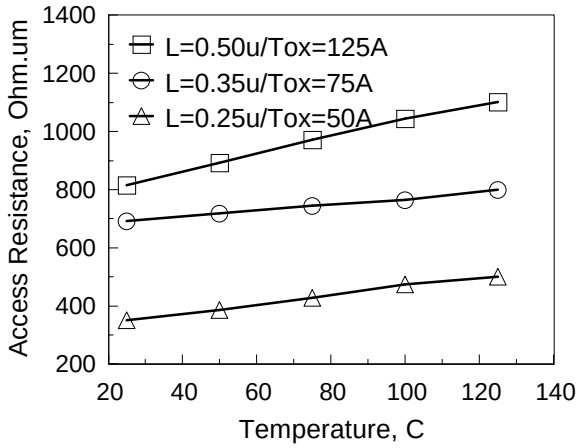

Figure 3. Measured access resistance values for Nchannel devices for three technologies.

Figures 4 and 5 show typical final model predictions comparted to the measured data for a 0.25µ device. The model is utilizing MM9 and accurate values of Rs and Rd. Similar accuracies are seen for all geometries and temperatures of interest. To see the effect of gate-induced mobility degradation on the device performance, the mobility related parameters in the model were set to 0. Results are discussed in 4.1.

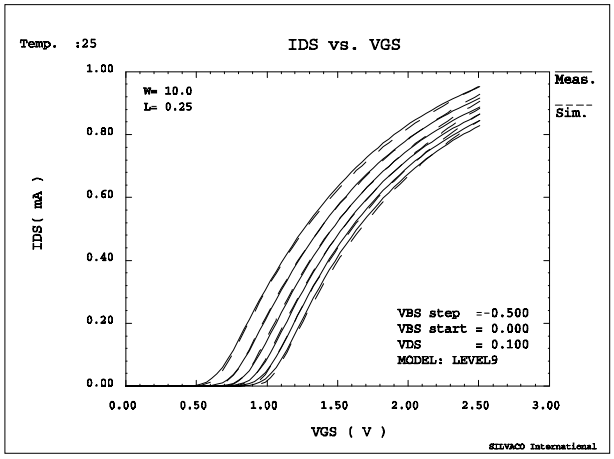

Figure 4. Measured data vs. model predictions in linear region.

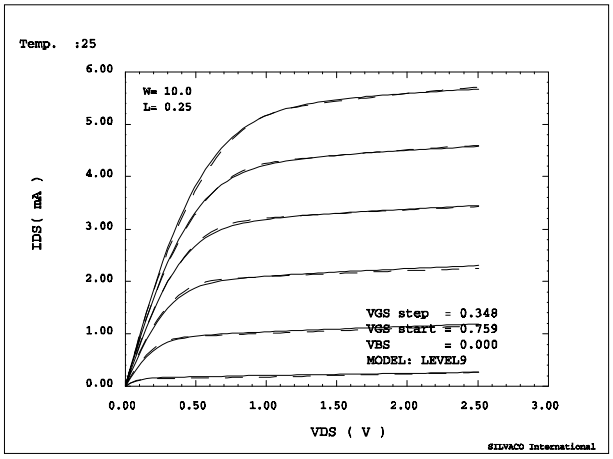

Figure 5. Measured data vs. model predictions in saturation region

4.1 CURRENT LOSS DUE TO MOBILITY DEGRADATION

Figures 6 & 7 show the simulated characteristics with disabled mobility degradation (effect of Vg) in the MM9 model. In each simulation, accurate Rs/Rd values demonstrated in Figure 2 and 3 were used. Figures 6 & 7 show the effect of gate-induced mobility degradation on the device characteristics in both linear and saturation regions. From similar simulations and comparison of the results with and without mobility degradation, the current degradation for each device from each technology was calculated. Results are in Figures 8 and 9. These Figures show the percentage current loss for each technology. Accordingly, this type of current loss is higher for thinner oxides, because of higher vertical fields. Current loss is

higher for electrons than holes, and its value is reduced with temperature.

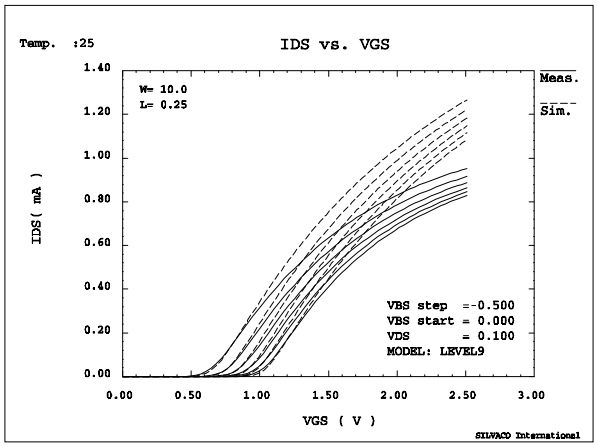

Figure 6. Model prediction with no mobility degradation compared with real measured data in linear region.

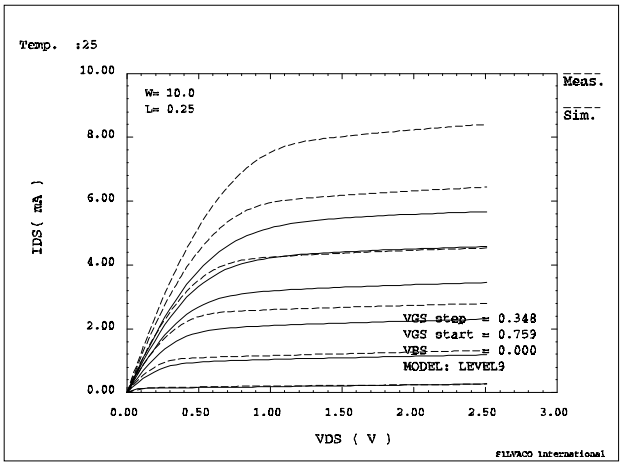

Figure 7. Model prediction with no mobility degradation compared with real measured data in saturation region.

It is seen that for the 0.50µ technology there is more than 25% current loss for the N-Channel and more than 21% loss for P-Channel devices due to gate-voltage-induced mobility degradation. This technology has a gate oxide thickness of 125 A. The calculated current loss does not include velocity saturation effects, which is another component of mobility degradation, not addressed in this work. The calculated current losses are higher for the 0.35µ and 0.25µ technologies that have gate oxide thicknesses of 75A and 50A respectively. For all three technologies, current loss is

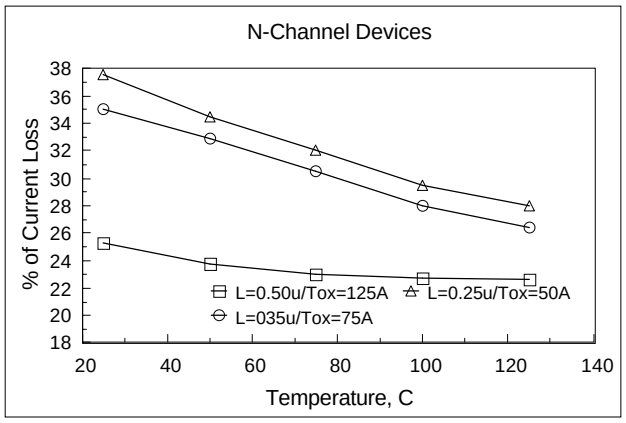

Figure 8. Percentage of current loss due to mobility degradation for N-Channel device of three Technologies

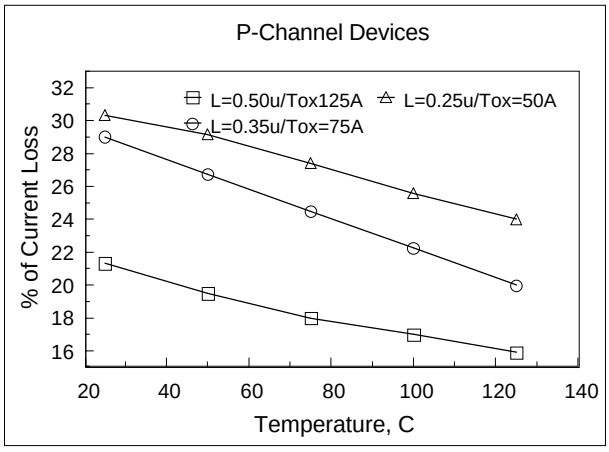

Figure 9. Percentage of current loss due to mobility degradation for P-Channel device of three Technologies

reduced at higher temperatures. This is, at least partly, due to an increase in the value of the access resistance with temperature, Figures 2 & 3. With higher Rs/Rd values, their contribution to current loss is more dominant.

5 CONCLUSIONS

The method involves the accurate development of a physical model with physically meaningful parameters for three submicron technologies. The physical model is used to calculate the current loss due to gate-voltage-induced mobility degradation for three gate oxide thicknesses. It is seen that current loss is increased for thinner oxide thicknesses and reduces at higher temperatures. Quantified results are presented.

REFERENCES

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