A Mathematical Model for the Threshold Voltage of a Partially and Fully Depleted MOS/SOI Structure with a Gaussian Distribution in the Film

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ABSTRACT

The analytical models for the electric field and potential distributions are necessary to establish the inversion or accumulation conditions at the front and back interfaces for a lot of SOI devices. The paper refers to a one-dimensional analysis, both for partially and fully depleted devices on films with non-uniform doping.

The goal of this paper is to obtain an accurate model of the electric field and potential distribution in the SOI capacitors with gaussian dependence of the doping profile in the film. In the fully depleted film case, the model takes into account the depletion of the silicon substrate. The model has been used for the threshold voltage computing, but they also represent a reference point in the development of news models for SOI-devices fabricated on gaussian profile films. The results were compared with PISCES numerical simulations and were in a good agreement.

Keywords: SOI films, Gaussian profile, Threshold voltage.

1 INTRODUCTION

In the latest years, the interest for SOI technologies increased at a rapid rate [1]. Sometimes, an additional doping of the film can be achieved simultaneously with the SOI layers fabrication, or separately, by a diffusion process. After this, a gaussian profile of concentration in the Si-film appears. Then a modelling of these structures becomes necessary. Lim and Fossum reported a unitary model, which accounts of front and back gates coupling both for uniform concentration in the film and for deep impurity implant in the film, approximated by a step profile [2]. For uniform impurity concentration in the film, a model that considers the depletion in the substrate in some particulars regimes were reported by Ravariu et all. [3].

The aim of this paper is to derive the expression of the electric field and potential in a Metal-Insulator-Silicon-Insulator-Substrate capacitor for a gaussian profile in fully- or partially- depleted films. This additional doping will influence the threshold voltage in order to avoid inversion at back/front interface.

The work hypotheses are:

- the neglect of the gate-body work function differences, interface charges and positive fixed charges in insulators.
- a one-dimensional analysis, considering the depletion approximation for the silicon film and eventual substrate.
- a uniform doping concentration in the substrate.
- p-type film and substrate.
- positives bias of the front gate and null potential (reference potential) on back gate.

The main notations are: $N_{A1}(x)$ - variable doping concentration in p-type film (after a diffusion process), N_{AS1} - surface doping concentration in p-type film, N_{A2} - doping in p-type substrate (constant), $x_{S1,S2}$ - film, respectively substrate thickness; $x_{d1,d2}$ - space charge region thickness in film, respectively in substrate; $x_{ox1,ox2}$ - thickness of front oxide, respectively of buried oxide; ε_{Si} - dielectric permittivity of silicon, ε_{ox} - dielectric permittivity of oxide, V_G - front gate voltage; ϕ_{F1} - Fermi potential at the surface of the film.

After a diffusion process in the SOI film, the impurity concentration looks like a gaussian function:

$$N_{A1}(x) = N_{AS1}\ ?\exp\left(-\frac{x^2}{4Dt}\right) \tag{1}$$

where D is diffusion coefficient, t - diffusion time, x - the distance into the film.

2 THE MATHEMATHICAL MODEL FOR THE THRESHOLD VOLTAGE

2.1 Partially Depleted Films

A slice from a MOS/SOI partially depleted structure is shown in figure 1. If the front gate will be positive biased, than a space charge region appears in the film, which will advance from 0 to x_2 with the V_G increasing. The electric field and potential distribution are derived by

Poisson's equation integration. In order to integrate this equation it will use the properties of the erf function.

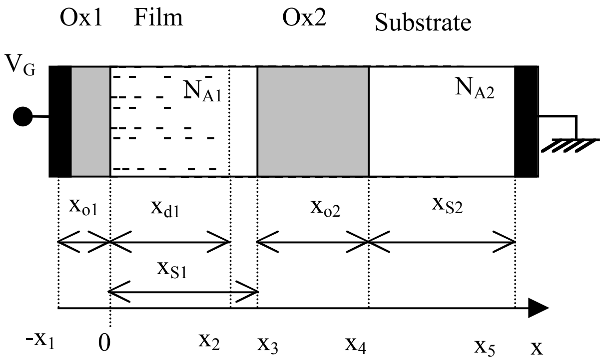

Figure1: Partially depleted structure.

The following field and potential distribution results:

For $x > x_2$, $E(x) = 0,\ V(x) = 0$ (2)

For $x \in (0, x_2)$, in the film,

$$E(x)=\frac{qN_{AS1}}{\varepsilon_{Si}}\cdot\sqrt{\pi Dt}\cdot\left[erf\,\frac{x_{d1}}{2\sqrt{Dt}}-erf\,\frac{x}{2\sqrt{Dt}}\right] \tag{3}$$

$$V(x)=\frac{qN_{AS1}}{\varepsilon_{Si}}\cdot x\sqrt{\pi Dt}\cdot\left[erf\left(\frac{x}{2\sqrt{Dt}}\right)-erf\left(\frac{x_{d1}}{2\sqrt{Dt}}\right)\right]+$$
$$+\frac{qN_{AS1}}{\varepsilon_{Si}}\cdot 2Dt\cdot\left[exp\left(\frac{-x^2}{4Dt}\right)-exp\left(\frac{-x_{d1}^2}{4Dt}\right)\right] \tag{4}$$

For $x \in (-x_1, 0)$, in the front insulator

$$E(x)=\frac{qN_{AS1}}{\varepsilon_{ox}}\cdot\sqrt{\pi Dt}\cdot erf\,\frac{x_{d1}}{2\sqrt{Dt}} \tag{5}$$

$$V(x)=-\frac{qN_{AS1}}{\varepsilon_{ox}}\cdot x\sqrt{\pi Dt}\cdot erf\,\frac{x_{d1}}{2\sqrt{Dt}}+$$
$$+\frac{qN_{AS1}}{\varepsilon_{Si}}\cdot 2Dt\cdot\left[1-exp\left(-\frac{x_{d1}^2}{4Dt}\right)\right] \tag{6}$$

The extension of the depletion region in the film results from (4):

$$x_{d1}=\sqrt{4Dt\cdot ln\,\frac{1}{1-\Phi_{S1}\cdot\frac{\varepsilon_{Si}}{2DtqN_{AS1}}}} \tag{7}$$

where ϕ_{S1} is the film surface potential. The threshold voltage can be defined like the gate voltage for which the film surface potential is $2\phi_{F1}$. It can be deduced from (2) - (6):

$$V_T = 2\Phi_{F1}+\frac{qN_{AS1}}{\varepsilon_{ox}}\cdot x_{ox1}\cdot\sqrt{\pi Dt}\cdot erf\,\frac{x_{d1max}}{2\sqrt{Dt}} \tag{8}$$

where ϕ_{F1} - Fermi potential at the surface of the film is:

$$\phi_{F1}=\frac{KT}{q}ln\,\frac{N_{AS1}}{n_i} \tag{9}$$

The maximum extension of the depletion region in the film, in threshold condition, x_{d1max}, can be derived from (7) for $\phi_{S1} = 2\phi_{F1}$.

2.2 The Condition of Fully Depleted Film

The condition of fully depleted film:

$$x_{S1} < x_{d1max}=\sqrt{\frac{2\varepsilon_{Si}}{qN_{A1}}\cdot 2\Phi_{F1}} \tag{10}$$

must be changed in respect with the maximum extension of the depletion region in the film, expressed by (7) in the condition of $\phi_{S1} = 2\phi_{F1}$.

Considering V_{GD} as the front gate voltage at which $x_{d1} = x_{S1}$, yields:

$$V_{GD}=\frac{qN_{AS1}}{\varepsilon_{ox}}\cdot x_{ox1}\sqrt{\pi Dt}\cdot erf\,\frac{x_{S1}}{2\sqrt{Dt}}+$$
$$+\frac{qN_{AS1}}{\varepsilon_{Si}}\cdot 2Dt\cdot\left[1-exp\left(\frac{-x_{S1}^2}{4Dt}\right)\right] \tag{11}$$

The MOS/SOI structure with $x_{S1} < x_{d1max}$ is: partially depleted for $V_G < V_{GD}$ and fully depleted for $V_G > V_{GD}$.

2.3 Fully Depleted Films

In the case of $V_G > V_{GD}$, due to the presence of buried oxide (see figure 2), the potential at x_3 abscissa becomes positive. Then a potential distribution across the substrate and implicitly a space charge region arises in substrate on x_{d2} distance, that will be derived in the following.

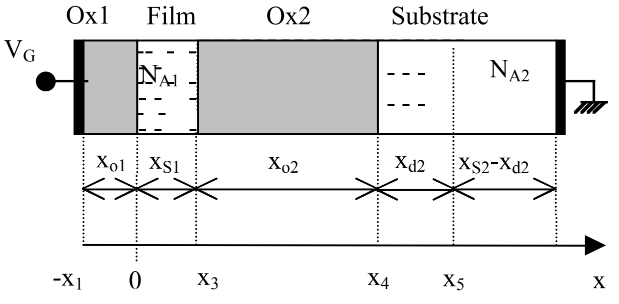

Figure 2: Fully depleted structure.

Following electric field and potential distributions result:
For $x > x_5$, in the neutral region of the substrate,

$$E(x) = 0, \quad V(x) = 0 \tag{12}$$

For $x \lfloor (x_4, x_5)$, in the depleted region of the substrate,

$$E(x) = \frac{qN_{A2}}{\varepsilon_{Si}} ?(x_{S1} + x_{ox2} + x_{d2} - x) \tag{13}$$

$$V(x) = \frac{qN_{A2}}{\varepsilon_{Si}} ?\frac{(x_{S1} + x_{ox2} + x_{d2} - x)^2}{2} \tag{14}$$

For $x \lfloor (x_3, x_4)$, in the buried insulator,

$$E(x) = \frac{qN_{A2}}{\varepsilon_{ox}} ?x_{d2} \tag{15}$$

$$V(x) = \frac{qN_{A2}}{\varepsilon_{Si}} ?\frac{x_{d2}^2}{2} + \frac{qN_{A2}}{\varepsilon_{ox}} ?x_{d2}(x_{S1} + x_{ox2} - x) \tag{16}$$

For $x \lfloor (0, x_3)$, in the depleted film,

$$E(x) = \frac{qN_{AS1}}{\varepsilon_{Si}} ?\sqrt{\pi Dt} ?\overline{\ } erf \frac{x_{S1}}{2\sqrt{Dt}} - erf \frac{x}{2\sqrt{Dt}} \Big) + \frac{qN_{A2}}{\varepsilon_{Si}} x_{d2} \tag{17}$$

$$\begin{aligned} V(x) = {} & \frac{qN_{A2}}{\varepsilon_{Si}} ?\frac{x_{d2}^2}{2} + \frac{qN_{A2}}{\varepsilon_{ox}} x_{d2} x_{ox2} + \frac{qN_{A2}}{\varepsilon_{Si}} x_{d2}(x_{S1} - x) + \\ & + \frac{qN_{AS1}}{\varepsilon_{Si}} ?x\sqrt{\pi Dt}\ \overline{\ } erf \frac{x}{2\sqrt{Dt}} - erf \frac{x_{S1}}{2\sqrt{Dt}} \Big) + \\ & + \frac{qN_{AS1}}{\varepsilon_{Si}} ?2Dt ? \exp \overline{=} \frac{x^2}{4Dt} \Big) - \exp \overline{=} \frac{x_{S1}^2}{4Dt} \Big) \end{aligned} \tag{18}$$

For $x \lfloor (-x_1, 0)$ in the front insulator,

$$E(x) = \frac{qN_{AS1}}{\varepsilon_{ox}} ?\sqrt{\pi Dt} ?erf \frac{x_{S1}}{2\sqrt{Dt}} + \frac{qN_{A2}}{\varepsilon_{ox}} x_{d2} \tag{19}$$

$$\begin{aligned} V(x) = {} & \frac{qN_{A2}}{\varepsilon_{Si}} ?\frac{x_{d2}^2}{2} + \frac{qN_{A2}}{\varepsilon_{ox}} x_{d2}(x_{ox2} - x) + \\ & + \frac{qN_{A2}}{\varepsilon_{Si}} x_{d2} x_{S1} + \frac{qN_{AS1}}{\varepsilon_{ox}} ?x\sqrt{\pi Dt} ?erf \frac{x_{S1}}{2\sqrt{Dt}} + \\ & + \frac{qN_{AS1}}{\varepsilon_{Si}} ?2Dt ? 1 - \exp \overline{=} \frac{x_{S1}^2}{4Dt} \Big) \end{aligned} \tag{20}$$

The gate voltage results as a sum of the potential drops over the front oxide, V_{ox1}, the silicon film, V_{S1}, the buried oxide, V_{ox2} and the substrate, V_{S2}:

$$V_G = V_{ox1} + V_{S1} + V_{ox2} + V_{S2}, \tag{21}$$

where:

$$\begin{aligned} V_{ox1} &= \frac{qN_{A2}}{\varepsilon_{ox}} ?x_{d2} ?x_{ox1} + \frac{qN_{AS1}}{\varepsilon_{ox}} x_{ox1} \sqrt{\pi Dt} ?erf \frac{x_{S1}}{2\sqrt{Dt}} \\ V_{S1} &= \frac{qN_{A2}}{\varepsilon_{Si}} ?x_{d2} ?x_{S1} + \frac{qN_{AS1}}{\varepsilon_{Si}} ?2Dt\ \overline{\ } 1 - \exp \overline{=} \frac{x_{S1}^2}{4Dt} \Big)\Big) \\ V_{ox2} &= \frac{qN_{A2}}{\varepsilon_{ox}} ?x_{d2} ?x_{ox2} \\ V_{S2} &= \frac{qN_{A2}}{\varepsilon_{Si}} ?\frac{x_{d2}^2}{2} \end{aligned} \tag{22}$$

It can observe that (21) and (22) represent a relationship between V_G and the extension of space charges region, x_{d2} in the substrate. This equation in respect with x_{d2} has real solution for the front gate voltage greater than depletion gate voltage, V_{GD}, delivered by (11).

The threshold voltage can be defined like the gate voltage for which the film surface potential is $2\phi_{F1}$. It can be deduced from (12) - (22):

$$V_T = 2\phi_{F1} + \frac{qN_{AS1}}{\varepsilon_{ox}} ?x_{ox1} \sqrt{\pi Dt} ?erf \frac{x_{S1}}{2\sqrt{Dt}} + \frac{qN_{A2}}{\varepsilon_{ox}} x_{d2} x_{ox1} \tag{23}$$

The dependence of the x_{d2} on V_G is given by:

$$\begin{aligned} x_{d2} = {} & -x_{SOI} + \ x_{SOI}^2 - \frac{N_{AS1}}{N_{A2}} ?4Dt ? 1 - \exp \overline{=} \frac{x_{S1}^2}{4Dt} \Big) - \\ & - 6 \frac{N_{AS1}}{N_{A2}} x_{ox1} \sqrt{\pi Dt} ?erf \overline{\ } \frac{x_{S1}}{2\sqrt{Dt}} \Big) + \frac{2\varepsilon_{Si}}{qN_{A2}} ?V_G ? ?^{1/2} \end{aligned} \tag{24}$$

where the notation x_{SOI} represents:

$$x_{SOI} = \frac{\varepsilon_{Si}}{\varepsilon_{ox}} ?(x_{ox1} + x_{ox2}) + x_{S1} \cup 3 ?(x_{ox1} + x_{ox2}) + x_{S1} \tag{25}$$

In this case too, the value of x_{d2} is real and positive (has physical sense), if it is fulfilled the conditions of "fully depleted film", that is: $x_{S1} < x_{d1max}$, where x_{d1max} is delivered by (7) with $\phi_{S1} = 2\phi_{F1}$, for gaussian profile in a SOI film.

3 SIMULATION RESULTS

The present analytical model was compared with numerical simulations made with PISCES simulator. The simulated structure is presented in figure 3. The simulations started from some experimental data [2]: SOI-MOSFET with x_{ox1}=0.1µm, x_{S1}=0.5µm, x_{ox2}=1µm, x_{S1}=1µm, N_{A2}=2*10^{15}cm^{-3} and the film had a gaussian profile from N_{AS1} =2*10^{16}cm^{-3} at the surface through 2*10^{15}cm^{-3} at the back interface. The mesh in the film was rafined to highlight the situation without depletion approximation. Figure 4 presents a comparision of the analytical models with numerical simulations for the above structure for front gate voltages in the range 0.8V … 1.2V (the field picture didn't comprise the components from front oxide due to the scale). The results are in a good agreement. The small differences come from depletion approximation used in the analytical model.

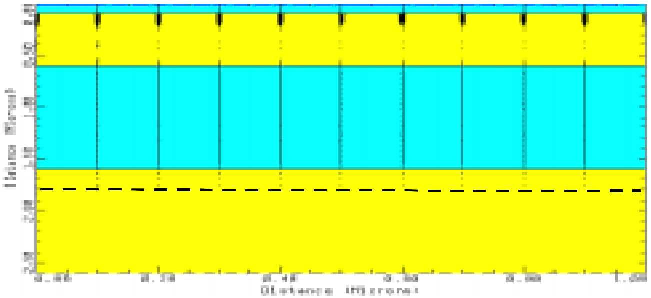

Figure 3: The simulated structure for V_G=8V (dotted line is the edge of the depletion region in the substrate).

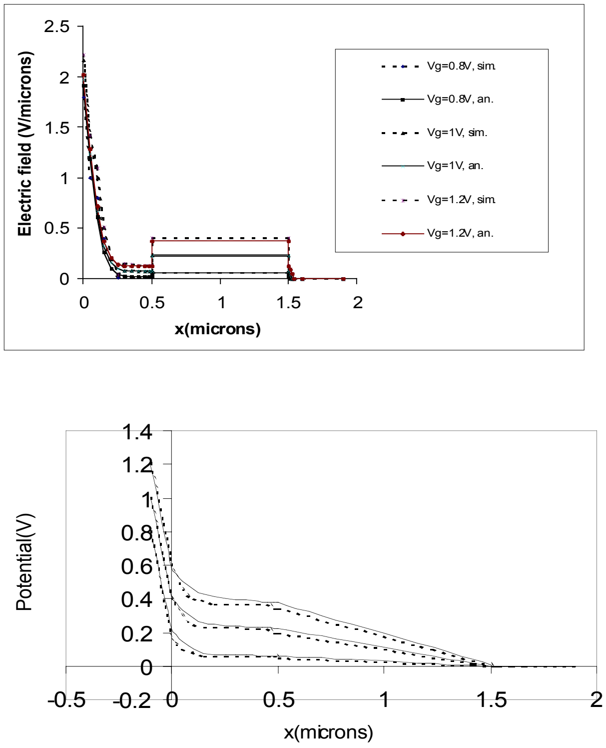

Figure 4: Electric field and potential distribution in the structure with gaussian profile in the film for V_G=0.8, 1, 1.2V (cont - analytical, dotted - simulated).

4 DISCUSSIONS

The threshold voltage was computed by three methods: (1) PISCES simulations; (2) the actual model according with eq.(23); (3) a simplified model [3] that considers a uniform average doping in the film≈5×10^{15}cm^{-3}.

A comparison between these results can be seen in table 1.

	Simulat.	**The actual model**	**The simplified model**
V_T	1.3V	1.39V	1.907V
Errors	0%	6.9%	46.7%

Table 1: Some threshold voltage values.

It can be observed that the presented model of the threshold voltage is closer to the simulation results than the simplified model (valid for uniform doping concentration).

5 CONCLUSIONS

An analytical model for the electric field and potential distributions in a Metal-Insulator-Silicon-Insulator-Substrate structure with a gaussian profile in fully- and partially- depleted films was presented. The analytical model was compared with PISCES simulations and was in a good agreement. The simulations have validated our initial hypothesis referring to the depletion of the substrate. The results of this paper represent an accurate manner of finding the threshold voltage and on the other hand a starting point for developing of new advanced models for SOI devices carried out on films with gaussian profile.

REFERENCES

[1]. S. Cristoloveanu and S. Li, "Electrical Characterization of Silicon-On-Insulator Materials and Devices", Kluwer Academic Publishers, 15-25, 1995.

[2]. H.K.Lim, J.G.Fossum - "Threshold voltage of thin-film silicon-on-insulator (SOI) MOSFET's", IEEE Trans. Electron. Devices, **ED-30**, 1244-1251, 1983.

[3]. C.Ravariu, et all. - "The influence of buried insulator type and film thickness on threshold voltage of a partially and fully depleted SOI-MOSFET", IEEE Int. Conf. on Semiconductors, 167-171,1999.