The 2.4F^2 Memory Cell Technology with Stacked-Surrounding Gate Transistor (S-SGT) DRAM

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ABSTRACT

This paper reports that the Stacked-Surrounding Gate Transistor (S-SGT) DRAM achieves a cell size of 2.4F^2. The S-SGT DRAM is structured by stacking several SGT-type cells in series vertically. In order to realize cell size of 2.4F^2, we propose the cell design of S-SGT DRAM.

By using proposed design, we demonstrate that the S-SGT DRAM can realize cell size of 2.4F^2 by process simulation, while cell size of conventional SGT DRAM is 4.8F^2. Therefore, the S-SGT DRAM is a promising candidate for future ultra high density DRAMs.

Keywords: SGT, S-SGT, DRAM, three-dimensional memory

1 INTRODUCTION

Recently, in normal DRAM, only capacitor structure has become three dimensional (3D) structure that is trench or stacked capacitor. However, in normal DRAM, it is difficult to keep cell size trend of DRAM. Therefore, the SGT DRAM [1] and NAND-structured DRAM [2] were proposed. However, these DRAMs do not use 3D space sufficiently. Therefore, the S-SGT DRAM [3],[4],[5] is proposed for ultra high density DRAM.

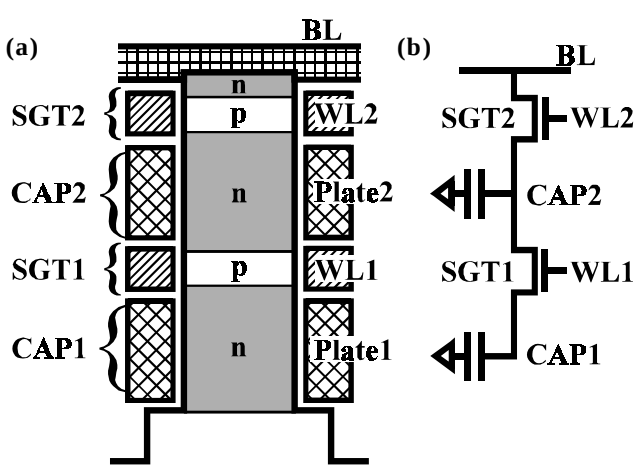


Fig.1(a): Structure of S-SGT DRAM,
(b): Equivalent circuit of S-SGT DRAM.

In this paper, a cell design of S-SGT DRAM is proposed that achieves a cell size of 2.4F^2 as shown by process simulation. In section 2, the design parameters of S-SGT DRAM are defined and the cell design of S-SGT DRAM is proposed. In section 3, cell size of S-SGT DRAM is discussed. In concrete, by using the proposed method, a S-SGT DRAM stacking 2 cells is designed, and the cell size of this device is discussed. In section 4, a S-SGT DRAM designed by proposed method is designed by process simulation [6]. And the cell size of the S-SGT DRAM is discussed. In section 5, this work is concluded.

2 THE CELL DESIGN OF S-SGT DRAM

2.1 Design parameters

The structure of S-SGT DRAM and the equivalent circuit are shown in Fig.1(a) and Fig.1(b), respectively. The S-SGT DRAM is structured by stacking several SGT-type cells in series vertically.

At first the design parameters of S-SGT DRAM are defined, which are necessary to design the S-SGT DRAM. And a functional dependence of the design parameters is formulated. The design parameters are defined as listed in Table1.

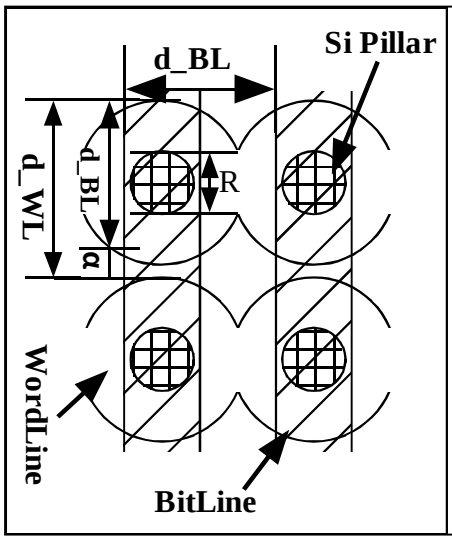
2.2 Cell design of S-SGT DRAM

In the proposed design, the dependence of the design parameters, which minimizes the cell size of S-SGT DRAM, are formulated for the first time.

The cell design of S-SGT DRAM is as follows.

R	Si pillar diameter (minimum feature size)
n	number of cells in one S-SGT DRAM
X	Difference radius between upper cell's SGT radius and lower cell's SGT radius
d_BL	bit-line pitch
d_WL	word-line pitch
α	$\alpha = d\_WL - d\_BL$
β	Isolation pitch

Table1: Design parameter definition.



$$S(n) = \frac{d\_BL \times d\_WL}{n} = \frac{2(R/2 + nX + \beta/2) \times 2[(R/2 + nX + \beta/2) + \alpha]}{n} = \frac{R^2 + R\alpha + 2R\beta + \alpha\beta + \beta^2}{n} + 4X^2 n + (4RX + 4X\beta + 2X\alpha) \quad (1)$$

Fig.2: Top-view of S-SGT DRAM and Equation (1).

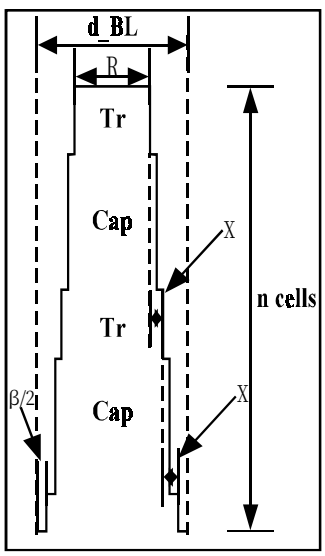


Fig.3: Cross-sectional view of S-SGT DRAM

S(n) is defined as one cell size of S-SGT DRAM stacking n cells. Fig.2 and Fig.3 show the top-view and cross-sectional view of S-SGT DRAM, respectively. In Fig.2, "R" is the Si pillar diameter. "d_WL" is word-line pitch and "d_BL" is bit-line pitch. "β" is the isolation pitch. And "α" is defined as the difference between "d_WL" and "d_BL". The word-line pitch is longer than the bit-line pitch for separating each word-line. Thus the Si pillars are located like rectangular mesh.

The cell size of S-SGT DRAM (S(n)) is given by Eq.(1) in Fig.2. Because a S-SGT DRAM is stacking n cells, S(n) is given by (d_WL×d_BL) divided by the number of stacking cells n.

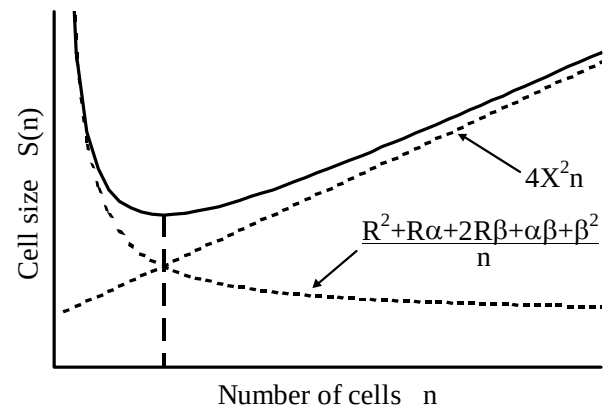


Fig.4: Variation of cell size of S-SGT DRAM (S(n)) as a function of number of cells (n) in one S-SGT DRAM.

Fig.4 shows a schematic view of Eq.(1) [Fig.2] representing the dependence between cell size of S-SGT DRAM (S(n)) and number of cells (n) in one S-SGT DRAM. The dotted lines indicate first term and second term of Eq.(1), respectively. The solid line indicates Eq.(1). It is found that the cell size of S-SGT DRAM (S(n)) is minimized at a certain number of cells (n) in one S-SGT DRAM. Therefore, it is required to find a function, which minimizes S(n).

In order to find a dependence of parameters, which minimizes S(n), $\partial S(n)/\partial n=0$ is solved. This dependence of parameters is formulated as follows.

$$X(n) = \frac{\sqrt{R^2 + R\alpha + 2R\beta + \alpha\beta + \beta^2}}{2n} \quad (2)$$

Here, X is the difference radius between upper cell's SGT radius and lower cell's SGT radius. It is found that X(n) is derived from Eq.(2) if SGT silicon pillar diameter (R),

number of cells (n) in one S-SGT DRAM, isolation pitch β and α are given.

However, word-line pitch (d_WL) and bit-line pitch (d_BL) are limited by design rule considerations and must satisfy Eq.(3).

$$d\_BL = R + 2nX + \beta \geq 2F \qquad (3)$$

Both equations define the design rule of the S-SGT cell for minimizing the cell size.

3 CELL SIZE OF S-SGT DRAM

Cell size of S-SGT DRAM is discussed by the proposed design method as shown in section 2. In order to compare to a conventional SGT DRAM, a 0.5μm design rule is considered. A conventional SGT DRAM cell has a cell size of $4.8F^2$. The silicon pillar diameter R of S-SGT DRAM is set to 0.5μm, while α and β are set to 0.2μm to 0.1μm, respectively.

Fig.5 shows the difference radius (X) between upper cell's SGT radius and lower cell's SGT radius as a function of number of cells (n) in one S-SGT DRAM for a 0.5μm design rule. In Fig.5 the design value X is derived from Eq.(2). It is found that when number of cells (n) in one S-SGT DRAM is increased it is necessary to decrease X.

Fig.6 shows the cell size of S-SGT DRAM (S(n)) as a function of number of cells (n) in one S-SGT DRAM for a 0.5μm design rule. Moreover, the design parameters X are shown. The x axis indicates number of cells (n) in one S-SGT DRAM. The left y axis indicates the cell size of S-SGT DRAM (S(n)), and right y axis indicates the design parameter X. The solid line indicates S(n) and the dotted line X. The line of $4.8F^2$ in Fig.6 indicates the cell size of one conventional SGT DRAM.

In Fig.6, S-SGT DRAM achieves a cell size of $2.4F^2$ in case of one unit stacking 2 cells and of $1.93F^2$ in case of one unit stacking 4 cells, if the design parameter X is chosen to 866Å. However when X is chosen to 866Å, the cell size of S-SGT DRAM stacking 16 cells (n=16) is larger than the cell size of S-SGT DRAM stacking 2 cells (n=2) as shown in Fig.6. However if X is appropriately chosen to 217Å, the cell size of S-SGT DRAM is further reduced. It is made clear that a cell size of S-SGT DRAM can be successively reduced even if the number of cells (n) in one S-SGT DRAM is increased.

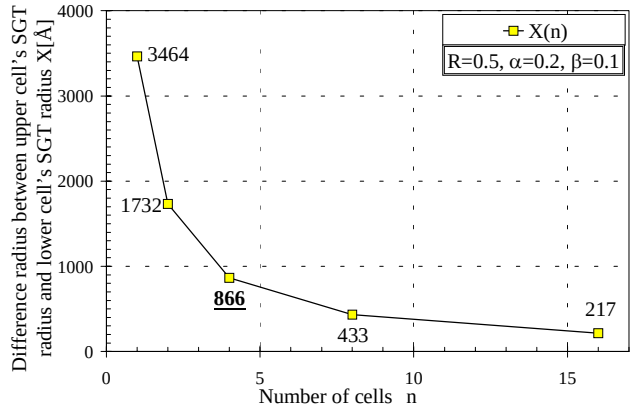


Fig.5: Difference radius between upper cell's SGT DRAM and lower cell's SGT DRAM X.

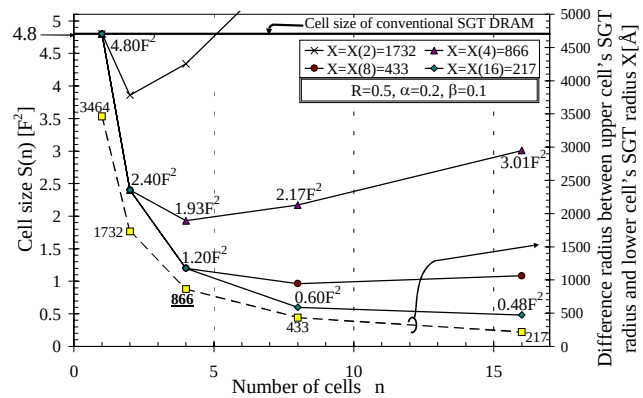


Fig.6: Cell size per bit of S-SGT DRAM.

4 $2.4F^2$ MEMORY CELL

A S-SGT DRAM designed by the proposed design method is fabricated by process simulation. At first Si pillar is formed. Secondary plate and word-line of lower cell are fabricated and upper memory cell is fabricated.

Fig.7 shows the process simulation results of S-SGT DRAM stacking 2 cells in word-line direction. The design parameters used in the simulation are listed in Table2. In Fig.7 the bit-line pitch is 1μm. Therefore the bit-line pitch is 2F, and the word-line pitch is 1.2μm. Thus, the cell size of S-SGT DRAM in Fig.7 is given as follows.

$$2F \times 2.4F \div 2 = 2.4F^2 \qquad (4)$$

As a result, it was found by process simulation that the S-SGT DRAM can realize cell size of $2.4F^2$.

In this section, a S-SGT DRAM designed by proposed method is fabricated by process simulation. And a memory cells of $2.4F^2$ was fabricated.

Design rule	0.5μm
Si pillar diameter R	0.5μm
Number of cells in one S-SGT DRAM (n)	2
Difference radius between upper cell's SGT radius and lower cell's SGT radius (X)	866 Å
Bit-line pitch d_BL	1μm
α	0.2μm
SGT oxide thickness	20nm
SGT height	1μm
Cell capacitor dielectric thickness (equivalent oxide thickness)	5nm
Storage capacitance	30fF

Table2: Design parameters of S-SGT DRAM of Fig.5.

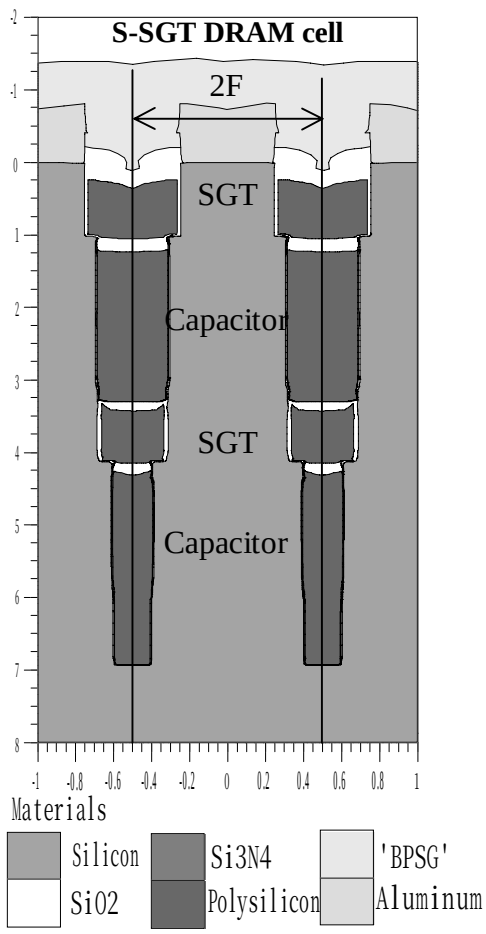


Fig.7: Process simulation result of S-SGT DRAM.

5 CONCLUSION

In this paper, we propose the cell design for S-SGT DRAM. By using proposed design, we demonstrated that the S-SGT DRAM achieves a cell size of $2.4F^2$ by process simulation, while cell size of conventional SGT DRAM is $4.8F^2$. S-SGT DRAM stacking several cells can drastically reduce cell size. Therefore, the S-SGT DRAM is a promising candidate for future ultra high density DRAMs.

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