A Methodology for Modeling a Complex Geometry on Wafer from a Layout Data

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ABSTRACT

This paper reports a novel methodology and its application to the modeling of a complex 3D geometry on wafer from a layout data. Our modeling method comprises the steps of: drawing a mask layout; transforming the mask layout into a 3D structure by simulating the physical semiconductor process; and extracting device parameters by numerical technique. In order to estimate a 3D structure from the mask layout data, we performed a topography simulation comprising various depositions and etching process steps. A finite element method (FEM) has been employed for extracting device parameters in the 3D structure such as a cell capacitor and interlayer dielectric. A concave cylindrical DRAM cell capacitor with a minimum feature size of 0.25 μm was chosen as a test vehicle to check the validity of the simulation. In this work, 62 parasitic capacitance with 4 cell-capacitance were extracted from a stacked DRAM cell structure over a bit line.

Keywords: Interconnect, DRAM, Capacitance simulation, 3D FEM.

INTRODUCTION

As the chip density increases with micro-miniaturization, the number of interconnection metal and interlayer dielectric also increases accordingly. Furthermore, since the scaling of the device on wafer also reduces the area available for a cell capacitor, it is crucial to develop a scheme to increase the effective surface area of the cell capacitor. In order to implement a sufficient amount of cell capacitance value in a reduced cell area, a cell capacitor with three-dimensional geometry has been widely employed [1]. As a result, the capacitor structure is highly non-planar and the topology on the semiconductor becomes more complicated and the aspect ratio becomes larger and larger. Accordingly, a great deal of attraction has been made on how to simulate the sophisticated geometry on the substrate and to estimate device parameters like parasitic capacitance and resistance [2][3].

SIMULATION METHODS

In this work, we employed a solid modeling method to generate a complicated three-dimensional structure on the substrate, like DRAM cell capacitor, using mask layout and topography simulation. The following steps can be used to create the three-dimensional structure for simulation.

(1) Draw a mask layout and define a process recipe.
(2) Perform topography simulation with the mask layout data and the process recipe.
(3) Obtain 3D-transfer information from the result of the topography simulation.
(4) Transform the mask data into a mesh structure for simulation with the mask layout data and the 3D-transfer information.

A schematic diagram illustrating the workflow of our generating methodology is given in Figure 1.

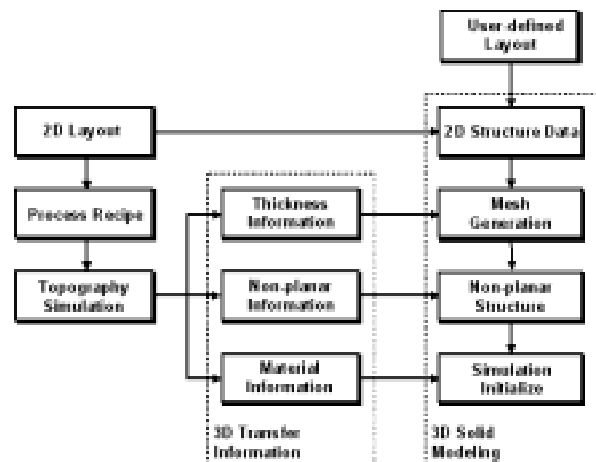


Figure 1: Schematic diagram illustrating the workflow.

Layout Editor and Run-Sheet Editor

Defining a three-dimensional structure is a challenging job. Moreover, the input processes are extremely time consuming and error-liable task. Therefore, as a general approach to define three-dimensional structure, layout editor and run-sheet editor are provided. Layout editor and run-sheet editor create the input data for topography simulation and solid modeling to generate a structure under investigation.

In order to generate sets of input data, layout editor includes the various operations such as rotation, translation,

scale, stretch and node edition. Figure 2 illustrates and example of layout.

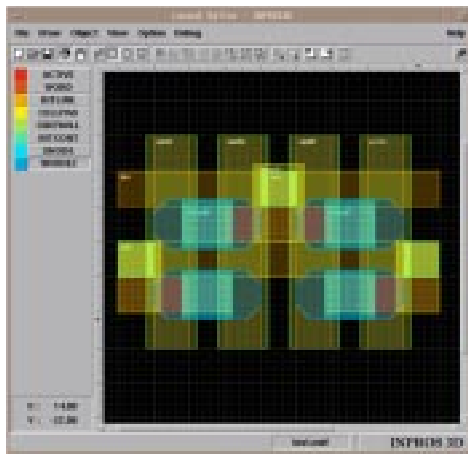


Figure 2: A plot showing the exemplary layout.

The structure to be simulated is obtained from the result of various deposition and etching processes. Run-sheet editor is used to handle process recipe. It can schedule process flow and conditions to generate the complex structure. As a mask layout data for topography simulation, run-sheet editor accepts files created by out layout editor. An example of process recipe is shown in Figure 3.

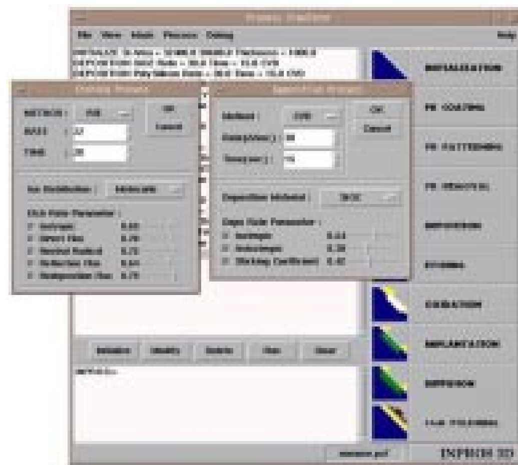


Figure 3: A plot showing the exemplary run-sheet for process recipe.

Numerical Method

Many numerical methods have been applied to extract the electrical parameters of the interconnect structure. These methods can be generally classified into two categories; charge integration method and energy calculation method. Charge integration method is to calculate the electric charge, assume constant potentials at the electrodes. Energy calculation method is to calculate the energy which is stored in the electric field between the conductors for given conductor voltages. Both energy calculation and charge integration method require the computational calculation of electric field, generally this uses finite differential method (FDM) and boundary element method (BEM) as a computational calculation method, and that uses finite element method (FEM).

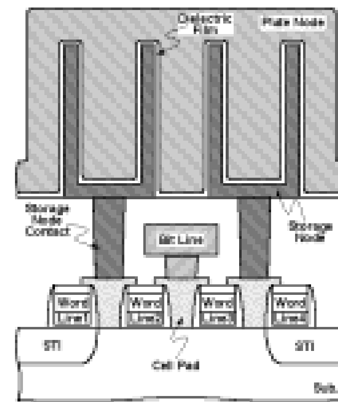
In this paper, energy calculation method has been employed for extracting capacitance in a complex VLSI structure such as a stacked DRAM cell. The governing equation needed for the calculation of capacitance is Laplace's equation, equation (1), derived from Maxwell's equation. Equation (1) can be formulated as equation (2).

$$?(\varepsilon(x,y,z)grad\phi(x,y,z))=0 \quad (1)$$

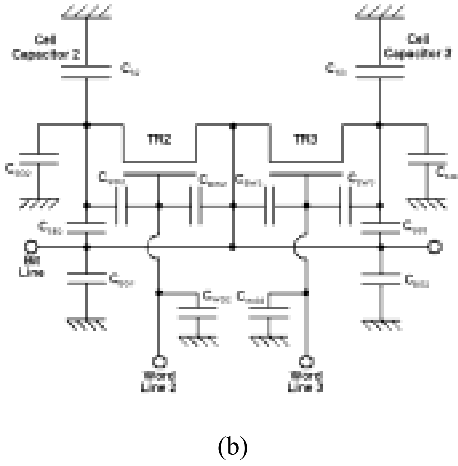
$$I=\varepsilon_0 \,{}_{V_D}\, \varepsilon(x,y,z)[(\frac{f\phi}{fx})^2+(\frac{f\phi}{fy})^2+(\frac{f\phi}{fz})^2]dV \quad (2)$$

From equation (2), the total electric field energy can be calculated in the investigated structure. And the total electric field energy for a given conductor voltages configuration can be expressed by sum of the energies stored in the parasitic capacitor. Therefore, the energy has to be calculated for different conductor voltage configuration equal to the number of existed capacitance. The parasitic capacitance values are obtained by solving the resulting linear system.

Figure 4(a) and 4(b) are schematic cross-sectional view illustrating a DRAM cell structure and its equivalent circuit diagram, respectively. Referring to Figure 4, the cross-sectional view include total 9 conductors consist of two storage nodes, four word lines, a bit line, a plate nodes and ground. Therefore, there are 36 unknown capacitance values, 2 cell capacitance values and 34 parasitic capacitance values. Since there are 36 unknown capacitance values, 36 different conductor voltage configurations are needed to calculate these capacitance.



(a)



(b)

Figure 4: (a) Schematic cross-sectional view illustrating a DRAM cell capacitor and (b) its equivalent circuit diagram.

The electric field energy at each voltage configuration is calculated by FEM. Equation (3) is the resulting linear system matrix.

$$\begin{bmatrix} U_{1,2}^{1} & U_{1,3}^{1} & \cdots & U_{8,9}^{1} \\ U_{1,2}^{2} & U_{1,3}^{2} & \cdots & U_{8,9}^{2} \\ \vdots & \vdots & \ddots & \vdots \\ U_{1,2}^{36} & U_{1,3}^{36} & \cdots & U_{8,9}^{36} \end{bmatrix} ? \begin{bmatrix} C_{1,2} \\ C_{1,3} \\ \vdots \\ C_{8,9} \end{bmatrix} = \begin{bmatrix} I^{1} \\ I^{2} \\ \vdots \\ I^{36} \end{bmatrix} \quad (3)$$

$$U_{i,j}^{k} = (\phi_i^k - \phi_j^k)^2 \quad (4)$$

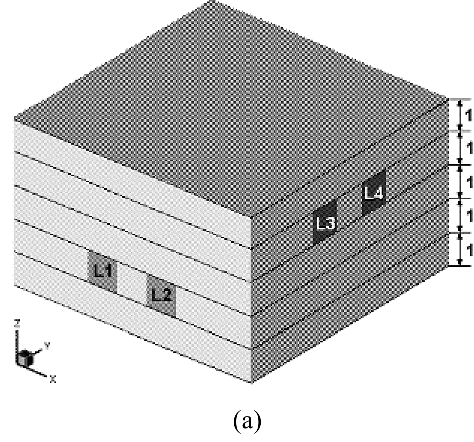
Where ϕ_i and ϕ_j are the potential values at the *i*-th and the *j*-th conductor, respectively. $C_{i,j}$ is the coupling capacitance between the *i*-th and the *j*-th conductor. Where index *k* means *k*-th voltage configuration. Therefore, where I^k is the calculated electric field energy obtained from equation (2) at *k*-th voltage configuration.

SIMULATION AND RESULTS

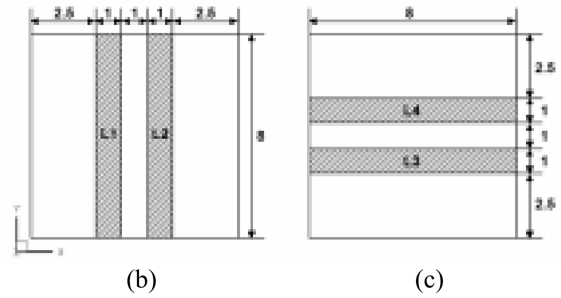
Firstly, we have used one of typical 3D interconnect structures for the verification of the result of our simulation. The result of calculation has been compared to the result of Ansoft's SPICELINK for same structure.

As shown in figure 5, the simulated structure has five dielectric layers. The dielectric constant and thickness of each layer is 3.9 and 1 µm, respectively. Two types of metal lines are embedded in dielectric layers, the width, thickness, and the length of each line is 1, 1, and 8 µm, respectively. It is assumed that the top and bottom planes of the simulation structure are grounded.

The capacitance matrices, equation (5) and (6), are used for comparing the result of each simulation. The (*i*, *i*) th diagonal element of matrix is called the total capacitance of



(a)



(b) (c)

Figure 5: Schematic overview of structure for simulation: (a) Thickness of each layer, (b) Dimension of the second layer, (c) Dimension of the fourth layer (unit:µm).

the *i*-th conductor, and is the sum of its capacitance to ground and its coupling capacitance with respect to all other conductors. The (*i*, *j*) the element is the negative of the coupling capacitance between the *i*-th and the *j*-th conductor. Equation (5) and equation (6) are the result of our simulation and one of SPICELINK [4], respectively. The result is in close agreement with an error of less than 5 percent.

$$\begin{bmatrix} 1.53 & -0.398 & -0.188 & -0.196 \\ -0.398 & 1.52 & -0.187 & -0.195 \\ -0.188 & -0.187 & 1.47 & -0.373 \\ -0.196 & -0.195 & -0.373 & 1.51 \end{bmatrix} \times 10^{-3}\, pF \quad (5)$$

$$\begin{bmatrix} 1.486 & -0.378 & -0.189 & -0.189 \\ -0.378 & 1.487 & -0.189 & -0.189 \\ -0.189 & -0.189 & 1.486 & -0.378 \\ -0.189 & -0.189 & -0.378 & 1.486 \end{bmatrix} \times 10^{-3}\, pF \quad (6)$$

Figure 6 shows a schematic view illustrating the generated DRAM structure. Referring to figure 6, four storage nodes with a capacitor dielectric and two parallel bit

lines are depicted over the four word lines on the substrate. The test vehicle includes four word lines, four storage nodes, two bit lines, a plate node, and a ground conductor. Therefore, 4 cell capacitances and 62 parasitic capacitances are existed in the structure.

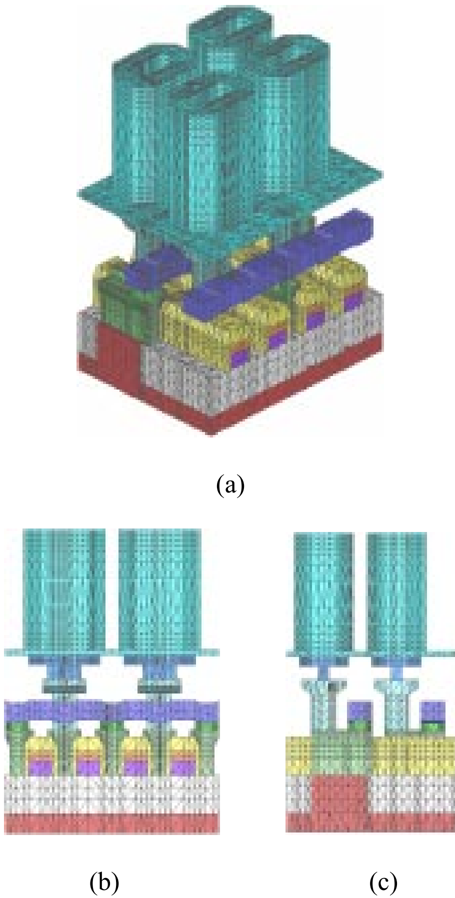


Figure 6: (a) Schematic view illustrating the simulated cell capacitor and schematic cross-sectional views alone (b) word line and (c) bit line.

Figure 7 is a schematic diagram illustrating the potential distribution of a DRAM cell capacitor when first word line and a first bit line are connected to 1 volt and the other conductors are grounded. The exemplary structure comprises four storage nodes with a dimension of $2.25 \times 1.75 \times 3.45\ \mu m^3$. The number of nodes for FEM calculation was 70,078 with 395,064 tetrahedron. The required CPU time for solving the potential distribution of the cell capacitor was approximately 25 minutes on ULTRA SPARC 10 workstation, while the swap memory for this calculation was 201MB.

Table 1 illustrates the values of various parasitic capacitances present in the conductors and interlayer dielectrics. In this calculation, we provided that the cell capacitance is 24 fF and the parasitic capacitance between storage node and word line is influential in parasitic capacitances.

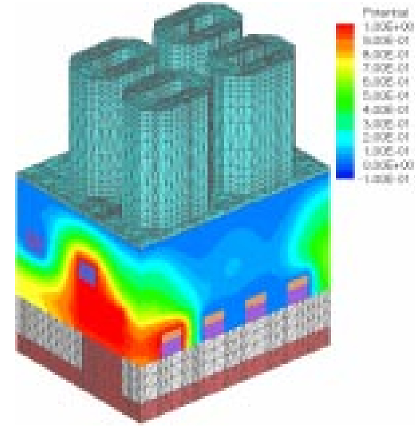


Figure 7: The potential distribution of a DRAM cell capacitor when first word line and first bit line are connected to 1 volt and the other conductors are grounded.

	W1	W2	W3	W4	B1	B2	STN1	STN2	STN3	STN4
W1		5.95e-2	6.44e-4	3.06e-5	4.35e-1	4.21e-2	2.04e-1	1.19e-4	2.01e-1	2.35e-5
W2			6.63e-2	6.64e-4	2.85e-2	4.17e-1	2.10e-1	4.62e-3	1.99e-1	5.31e-4
W3				5.99e-2	2.85e-2	4.18e-1	4.63e-3	2.08e-1	5.32e-4	1.98e-1
W4					4.35e-1	4.21e-2	1.19e-4	2.03e-1	2.35e-5	2.02e-1
B1						5.10e-2	1.76e-1	1.76e-1	1.46e-1	1.46e-1
B2							4.40e-4	4.40e-4	1.69e-1	1.69e-1
STN1								1.70e-2	1.88e-2	6.73e-4
STN2									6.73e-4	1.87e-2
STN3										7.84e-3
PLT	4.57e-4	3.35e-4	3.36e-4	4.57e-4	2.90e-2	5.20e-2	24.037	24.031	24.044	24.043
GND	6.57e-2	6.11e-2	6.11e-2	6.57e-2	5.90e-2	2.75e-2	1.20e-2	1.20e-2	1.20e-2	1.20e-2

Table 1: A table illustrating calculated capacitance present in the conductors and interlayer dielectrics (unit:fF).

CONCLUSIONS

In this paper, a concave cylinder type DRAM cell capacitor having Ta_2O_5 dielectric layer was investigated for simulating a complex geometry on wafer. As a result, we extracted 4 cell capacitance and 62 parasitic capacitance values and found that the parasitic capacitance between storage node and word line is influential in a stacked DRAM.

ACKNOWLEDGMENT

This work was supported by ‘A Collaborative Project for Excellence in Basic System IC Technology’ program from COSAR and research program 98-NE-03-05-A-01 from KISTEP

REFERENCES

[1] A. Nitayama et al., IEDM Tech. Dig., pp.355-358, 1998.
[2] K. Koyama et al., SSDM, pp.268-269, 1997.

[3] J. S. Yuan et al., VMIC, pp.410-412, 1990.
[4] W. Hong et al., IEEE Trans. Microwave Theory Tech., vol 46, No. 8, pp. 1037-1044, 1998.