Two-Dimensional MOSFET Dopant Profile by Inverse Modeling via Source/Drain-to-Substrate Capacitance Measurement

C.Y.T. Chiang*, Y.T. Yeow* and R Ghodsi**

*Department of Computer Science and Electrical Engineering
The University of Queensland, Brisbane, Qld, Australia 4072
Phone: +61-7-33654442 Fax: +61-7-33654999
email: ytchiang@netscape.net

**Cypress Semiconductor, San Jose, CA 95134

ABSTRACT

This paper proposes and demonstrates a new approach to 2-dimensional dopant profile extraction for MOSFET's by treating the source/drain-to-substrate junction as a gated diode. The small-signal capacitance of the diode measured as a function of gate and source/drain bias is used as the target to be matched in an inverse modeling process. It is shown that this capacitance allows both the substrate dopant profile in the channel region and the source/drain-to-substrate profile parallel to the surface to be evaluated with a single set of measurement data. Experimental results for n-MOSFETs with drawn channel length = 1 µm is presented. Comparison of other electrical measurement with simulation data based on the extracted profile is also given.

Keywords: MOSFET's, semiconductor device doping, semiconductor device measurements, semiconductor device modeling.

1 INTRODUCTION

The design and realization of an appropriate dopant concentration profile is critical in achieving the desired electrical characteristics of a modern MOSFET. An accurately determined dopant profile is also important for the calibration of process simulators. While many physico-chemical analysis techniques are now available for dopant profile extraction [1], they require extra chemical processing and data calibration. With advances in numerical device simulation, the inverse modeling technique using a particular set of experimental data has become popular for the extraction of MOSFET 2-D dopant profile: Khalil et al. applied this method to a combination of gate-to-source/drain capacitance (C_{gsd}) and drain/source-to-substrate junction (C_{sdb}) [2] and Lee et al. used I-V data in the subthreshold region [3]. In this method one or more measured electrical quantities of a device are chosen as the target data; numerical simulation is then carried out with an initial dopant profile for the device to calculate the corresponding electrical quantities. The assumed profile is then adjusted iteratively to obtain an optimal match of simulation data to their experimental target.

An inverse modeling process using only the capacitance of the drain/source-to-substrate junction (C_{sdb}) for extracting the complete 2-dimensional profile of MOSFET's is presented. We treat the junction as a gated diode under the control of gate bias and junction reverse bias. With channel in accumulation, the measured capacitance includes the depletion capacitance of the inner sidewall junction and is therefore a function the source/drain-to-substrate junction profile in a direction parallel to the surface. By sweeping the junction reverse bias and the channel to different levels of accumulation, we cause the depletion region of this sidewall junction to sweep to varying extent on both sides of the junction. By biasing the channel into inversion, the measured capacitance includes the inversion layer-to-substrate capacitance which is dependent on the substrate dopant profile in channel region [4]. Thus by measuring this capacitance over a suitable range of gate and source/drain bias, we would have captured the contributions to the measured capacitance from the dopant concentration of whole active region of the transistor ie where the field-effect action of the gate is active. In comparison, the gate-to-source/drain capacitance referred to in previous paragraph is more a function of the channel potential distribution along the surface arising from a given source/drain reverse bias. Its dependence on the surface dopant profile is through the fact that the dopant profile influences the channel potential distribution.

The nature of the gated diode is such that the contributions to the measured capacitance from the bottom and the outer sidewall junctions can be determined and subtracted from the measured data. Only the capacitance contributions from the inner sidewall junction and inversion layer-to-substrate junction are used as the target data in the inverse modeling process. This implies that the simulation work does not have to model the length of the experimental source and drain junctions or the outer sidewall junctions.

2 BASIS OF INVERSE MODELING

C_{sdb} has four components: $C_{sdb}=C_{invb}+C_{sdb1}+C_{sdb2}+C_{sdb3}$, inversion layer-to-substrate capacitance, inner sidewall capacitance, bottom capacitance and outer sidewall capacitance respectively, this is shown in Fig. 1.

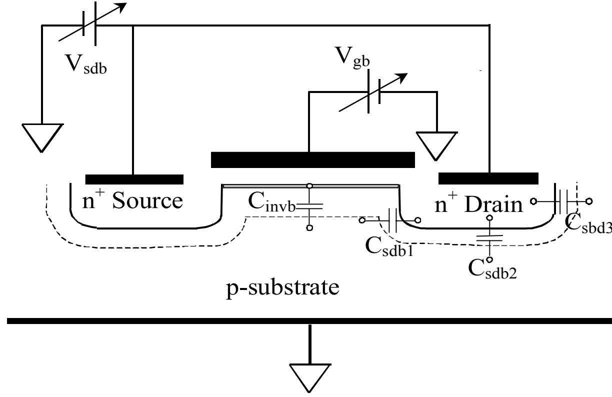

Fig. 1. Device bias for C_{sdb} measurement and components of C_{sdb}.

As we vary the gate bias, the carrier type and concentration in the channel region changes, and hence also the capacitances of the first two components which are associated with the channel region.

Fig. 2 shows the measured C_{sdb} as a function of gate-to-substrate bias V_{gb} and source/drain-to substrate reverse bias Vsdb for an n-channel LDD MOSFET (W/L = 50 μm/1μm, gate oxide = 15 nm). For a given gate bias, the measured capacitance decreases with increasing junction reverse bias due to the increase of the depletion widths of the individual components. It can also be seen that at $V_{gb} = 0$ V, corresponding to a depleted surface in the transistor channel, the capacitance shows a minimum for all V_{sdb}'s. As the channel goes into accumulation ($V_{gb} < 0$ V) the inner sidewall capacitance C_{sdb1} comes into existence and the measured capacitance increases due to reduction of the depletion width of this sidewall junction with increasing degree of accumulation. In inversion ($V_{gb} > 0$ V) the increase in the measured capacitance is due to the introduction of the inversion layer-to-substrate capacitance C_{invb} which very rapidly saturates to a level corresponding a fixed substrate depletion width (at the given source/drain reverse bias). C_{invb} and C_{sdb1} are functions of the channel region substrate and source/drain junction dopant profiles to be extracted as well as functions of the gate-to-substrate bias V_{gb} and the source/drain-to-substrate bias V_{sdb}. Their sum, ($C_{invb} + C_{sdb1}$) is chosen as the target experimental data in our inverse modeling.

When the gate bias is such that the channel region is depleted, both the above components disappear: C_{invb} because the inversion layer is absent, C_{sdb1} because the substrate next to the sidewall is completely depleted. Detailed examination of this raw measured C_{sdb} as a function of V_{gb} in Fig. 2 reveals that this capacitance has a very "flat" minimum. This supports the argument that at the minimum capacitance point there are no contributions from the V_{gb}-dependent components C_{invb} and C_{sdb1}. This applies for the complete range of V_{sdb}, giving rise to the minimum capacitance line seen in Fig. 2. This minimum capacitance line therefore represents the remaining capacitance components, i.e. ($C_{sdb2} + C_{sdb3}$) which is a function of source/drain bias but not the gate bias. They are not of interest in our extraction process and are removed from the measured capacitance before applying inverse modeling. This is achieved by subtracting the minimum capacitance line from all other measured data to leave behind ($C_{invb} + C_{sdb1}$) as a function of V_{sdb} and V_{gb}. The results are shown in Fig. 3.

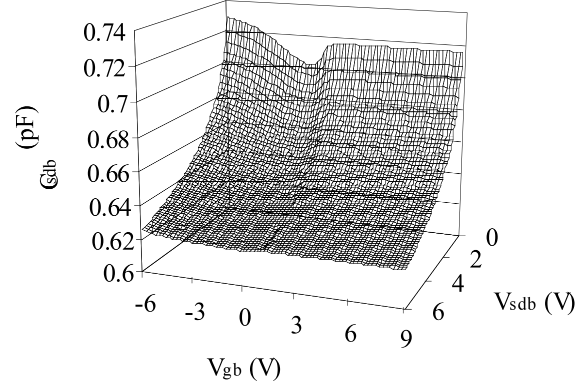

Fig. 2. 3-D plot of the measured C_{sdb} as a function of V_{gb} and V_{sdb}.

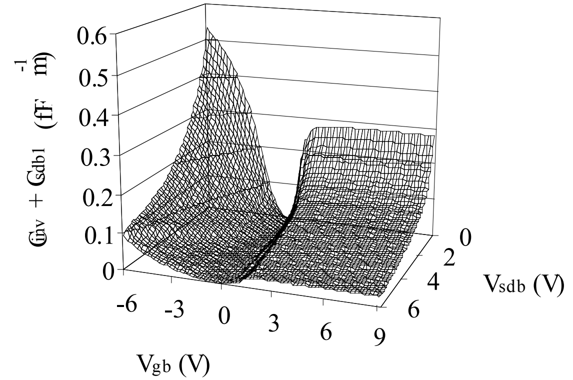

Fig. 3. ($C_{inv}+C_{sdb1}$) as a function of V_{gb} and V_{sdb} obtained from data in Fig. 2.

The dopant profile extraction process starts by building up a suitable dopant profile model for the MOSFET with a number of analytical profiles reflecting the various fabrication processes involved. Each analytical profile has its own set of adjustable parameters. A numerical device simulation program is then used to evaluate the gated diode capacitance for the assumed profile and then the parameters are adjusted to produce the best fit of the simulated capacitance to the measured data. For matching purposes, the experimental capacitance is reduced to per unit width quantity for compatibility with results of 2-D simulator. Similar subtraction process described in the treatment of experimental capacitance is used to remove the contributions of ($C_{sdb2} + C_{sdb3}$) in the simulation data.

Based on the knowledge of the fabrication processes of the devices under test, we have modeled our device thus: source/drain junction by two 2-D Gaussian profiles to account for LDD structure, the channel as two 1-D Gaussian profiles to account for threshold adjust and punch-through implants, and the substrate as a constant dopant concentration. The device simulator MEDICI [5] is then used to compute the simulation C_{sdb} as a function of V_{sdb} and V_{gb} and an optimization process is based on the Levenberg-Marquardt algorithm. Subtraction process described in the treatment of experimental capacitance is used to extract the simulation $C_{invb}+C_{sdb1}$. The best representation of the actual profile is obtained by adjusting the Gaussian profile parameters to produce the best fit between measured and simulated $C_{invb}+C_{sdb1}$.

3 MEASUREMENT

Fig. 4 shows the instrumentation used to obtain the results in Fig. 2. The HP4284A LCR meter was used to measure the capacitance and to apply the reverse bias between the source/drain and the substrate (V_{sdb}). Measurement signal was 50 mV at 100kHz injected into the substrate and detected at the grounded source and drain junctions. HP 4145A parameter analyzer was used to provide the necessary gate-to-source/drain bias.

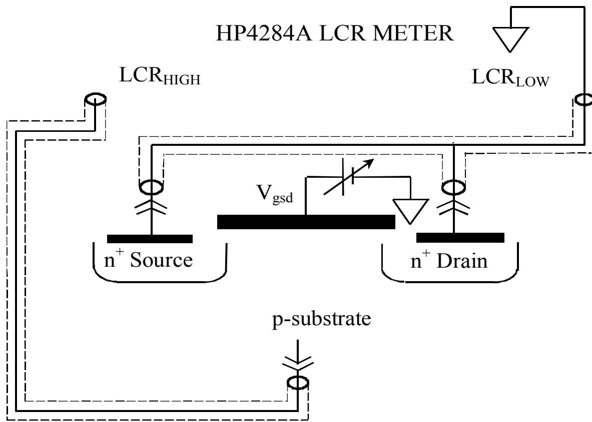

Fig. 4. Instrumentation for measurement of C_{sdb}.

4 RESULTS AND DISCUSSION

Fig. 2 shows the measured C_{sdb} as a function of V_{gb} and V_{sdb} for a LDD nMOSFET with estimated L_{eff}=0.75 µm (drawn W/L=50 µm/1µm, gate oxide=15 nm). Fig. 3 shows $C_{invb}+C_{sdb1}$ obtained from data in Fig. 2 by subtracting the minimum measured C_{sdb} at V_{gb}=0V. Our analytical profile models and associated adjust parameters are described in Table 1. The initial guess of each parameter was set to the middle of range set and the simulation capacitance C_{sdb} was calculated for the same bias range used in measurement. Device gate length was set to the same drawn length. Other device parameters such as gate material and work function

Region and Dopant Model type	Parameters	Range of Parameters
n^+ drain implant 2-D Gaussian	Distance of Gaussian peak from gate edge Gaussian Peak at surface y direction sigma Ratio of x direction sigma to y direction sigma	0.1 to 0.5 µm 1×10^{20} to 5×10^{20} cm^{-3} 0.1 to 0.3 µm 0.3 to 0.9
n-type LDD implant 2-D Gaussian	Distance of Gaussian peak from gate edge Gaussian peak at surface y direction sigma Ratio of x direction sigma to y direction sigma	−0.1 to 0.1 µm 1×10^{18} to 7×10^{18} cm^{-3} 0.1 to 0.3 µm 0.3 to 0.9
p-type threshold implant profile 1-D Gaussian	Gaussian peak at surface y-direction sigma	5×10^{16} to 1×10^{17} cm^{-3} 0.1 to 0.3 µm
p-type punch-through implant 1-D Gaussian	Gaussian peak Distance of peak from surface y-direction sigma	1×10^{16} to 5×10^{16} cm^{-3} 0.1 to 0.6 µm 0.1 to 0.3 µm
Uniform p-type substrate	Dopant concentration	1×10^{15} to 2×10^{16} cm^{-3}

Table 1. Description of Analytical Profiles Used in Inverse Modeling.

difference, which would affect the threshold voltage, were selected to reflect the experimental device. To optimize the parameters of the analytical models obtained, the simulator was programmed to run until the RMS error for the used 20 data is less than 5 %. Where necessary the range limits for the parameters were reset to ensure that the optimization process does not push a parameter to its range limit. Fig. 5 is the comparison of the experimental and simulation $C_{invb}+C_{sdb1}$ obtained after optimization. The agreement is within 5% set in the optimization process. Fig. 6 is the 3-D plot of the optimized profile.

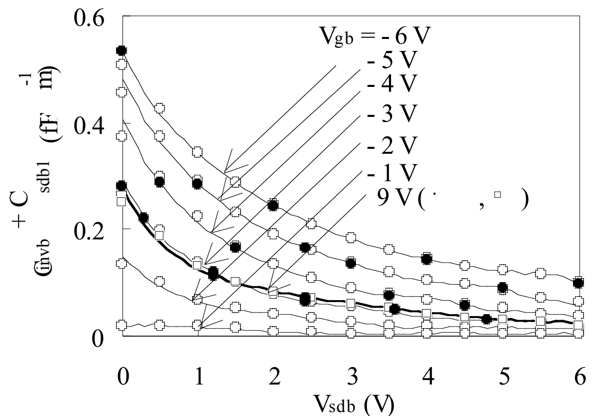

Fig. 5. Comparison of measured and simulation ($C_{invb}+C_{sdb1}$) per unit width as a function of V_{sdb} with V_{gb} as a parameter for the 1 µm device. Lines are experimental data, "○" and " " are simulation data. "•" are experimental points chosen as target data for inverse modeling.

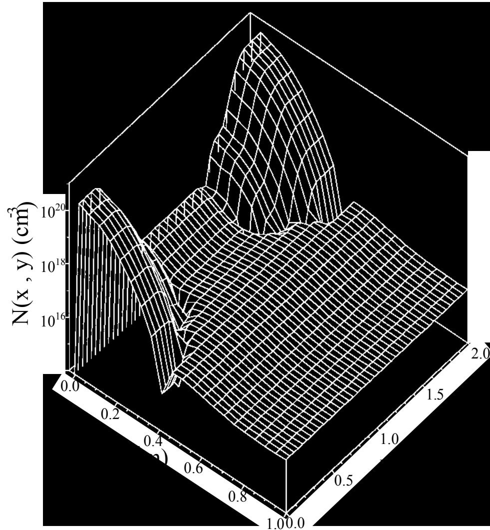

Fig. 6. 3-D plot of the extracted dopant profile. Device based on measured data in Fig. 3.

We also briefly investigated the effects of changes in some assumed device parameters on extracted profiles: 5% change in gate oxide thickness or gate length leads to a maximum of 10% change in the dopant concentration at the critical locations.

For validation, we compared the measured I_{ds}-V_{ds} (Fig. 7), the subthreshold current (Fig. 8) and the gate-to-drain capacitance (Fig. 9) with the simulation results obtained using the extracted profile. Two different mobility models

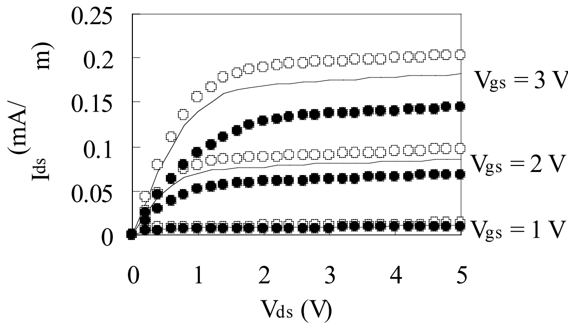

Fig. 7. Comparison of measured and simulation per unit width I_d-V_{ds} characteristics. Simulation uses the extracted profile of Fig. 6. Lines are experimental, "○" and "•" are simulation based on the mobility models including the surface field effect according to MOBA and MOBB respectively.

were tested. They account for dopant concentration dependence and longitudinal field dependence in the same way but have different surface-field dependence: MOBA in which only the inversion layer is affected by the transverse field and MOBB in which carriers at every position is affected the transverse field [5]. The comparison indicates that simulation results at low transverse fields and current agree well with measurement. At high drain currents the observed differences arise more from the difference in the mobility models than from accuracy of the extracted dopant profile.

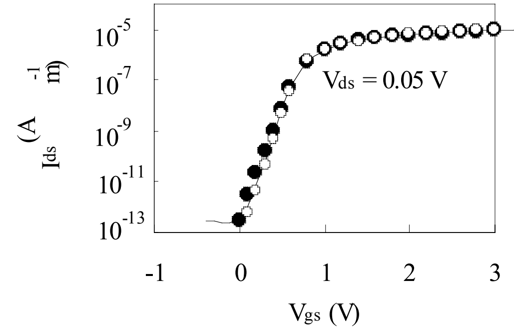

Fig. 8. Comparison of measured and simulation per unit width subthreshold I_d-V_{gs} characteristics. Simulation uses the extracted profile of Fig. 6.

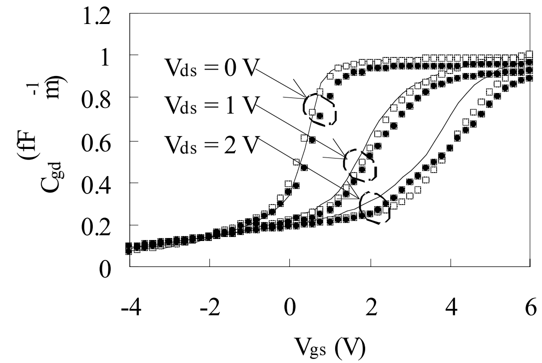

Fig. 9. Comparison of measured and simulation per unit width C_{gd}-V_{gs} characteristics. Simulation uses the extracted profile of Fig. 6.

5 CONCLUSIONS

We have demonstrated a new and simple method of MOSFET 2-D dopant profile extraction based on source/drain-to-substrate capacitance. Although the capacitances involved are small (0-20 fF), our subtraction process removes stray capacitances as well as the bottom and outer sidewall junction capacitances. As measurement there is no drain current flowing in the device, the simulation results and hence also the extracted dopant profile are independent of carrier transport model assumed in the simulation.

REFERENCES

[1] A.C. Diebold, M.R. Kump, J.J. Kopanski and D.G. Seiler, *J. Vac. Sci. Technol. B*, 14, pp. 196-201, 1996.

[2] N. Khalil, J. Faricelli and C.-L. Huang, *J. Vac. Sci. Technol. B*, 14, pp. 224-230, 1996.

[3] Z. K. Lee, M.B. McIlrath and D.A. Antoniadis, *IEEE IEDM. Tech. Dig*., p. 683-686, 1997.

[4] C.Y.T. Chiang, C.T.C. Hsu, Y.T. Yeow and R. Ghodsi, *IEEE Trans Electron Dev*. vol. ED-45, No. 8, pp. 1732-1736. 1998.

[5] MEDICI: *Two-Dimensional Device Simulation Program*, TMA Associates, Palo Alto, CA, 1994.