Modelling of the "Gated-Diode" Configuration in Bulk MOSFET's

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ABSTRACT

A study of the "gated-diode" configuration in MOSFET's for characterising hot-carrier degradation by employing 2-D simulations is presented in this paper. We use both process and device simulations to understand operational sensitivity of this technique. The parameters involved in the gated-diode measurement like recombination processes and carrier concentrations, which are not available from experiments, will be discussed. The interface trap distribution across the bandgap and spatial distribution are also explored here. In addition, the gated-diode measurement method is modelled with specific task of determining interface state density.

Keywords: MOSFET, hot-carrier effects, interface traps, gated-diode, simulation.

1 INTRODUCTION

The basic building block of dominant CMOS technology today has evolved to a channel length below 0.25μm. Due to the high electric field, hot-carrier effect in these devices is an important reliability issue. The hot-carrier effects create a damaged region at oxide-silicon interface which affects device performance and long term reliability. Moreover, to gain further insight into the electrical characteristics of sub-micrometer MOSFET's, it is mandatory to obtain the interface-state distribution across the energy bandgap[1]. The spatial distribution of the interface traps and the nature of the traps are also crucial in this study. The gated-diode technique is useful in obtaining quantitative information about the traps

MOSFET's connected in gated-diode configuration which is also better known as the gated-diode technique, as a means to study surface/interface effects was first described by Grove[2] in 1966. The technique specifically gives quantitative information on interface quality. Later on, this technique has been employed to characterise[3-6] the physical damage induced by hot-carrier effects.

This technique involves applying a range of bias to the gate sweeping the channel from accumulation to inversion, while source and drain are either kept at a small reverse[6] or forward[3-5] voltage. A typical setup of this measurement is depicted in Fig 1. The gated-diode current is the measured drain current in this configuration. Several experimental works[3-6] have provided insights into this hot-carrier characterisation technique.

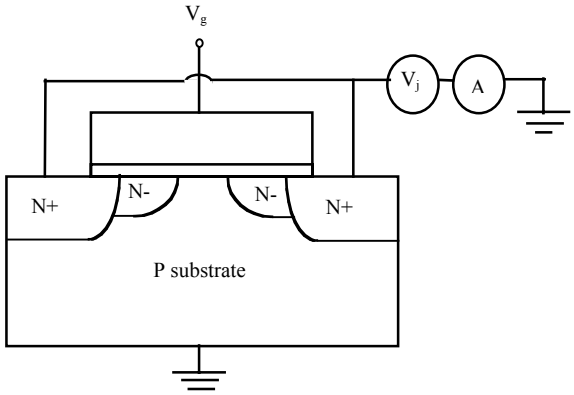

Fig 1 Schematic diagram of gated-diode setup.

The principle of measurement behind this method is based on the changes in the gate voltage, V_g, that will control the rate of recombination at the interface by changing the position of the surface depletion region. When V_g is swept from inversion threshold, through depletion into increasingly strong accumulation, the effective zone moves like a pointer of decreasing width along the interface towards the drain. Finally, it will move away from the gate and completely separate from the SiO_2/Si interface. For hot-carrier damage characterisation, the interface traps probed by the "pointer" will give rise to peaks (due to additional recombination at the interface traps).

2 SIMULATIONS

In the simulations, a configuration in Fig 1 is defined. The source and drain were short-circuited to avoid any potential drop along the channel. A voltage V_j is applied to the source/drain junction to forward bias the source/drain-substrate junction. The current is then measured as a function of gate bias. Here, the forward "gate-diode" method is chosen because of it's higher sensitivity. The n-channel MOSFET used for the simulation process is imported from the process simulator, T-SUPREM4[7]. The technology file for the nMOSFET is supplied by a local foundry. The actual gate-LDD overlap region of the simulation structure is shown in Fig 2. The simulation

device used is an LDD device, with N+ poly gate. The metallurgical channel length is 0.7μm and gate oxide thickness is 13.5nm. In order to obtain a more realistic simulation of a degraded device, we have introduced a continuous interface trap density of 1 X 10^{12} $cm^{-2}eV^{-1}$ extending from the channel into the LDD region.

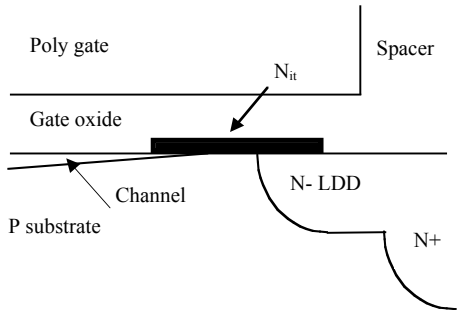

Fig 2 Cross-sectional view of the relative position of interface traps and fixed charge over the channel and in the gate-LDD overlap of the MOSFET.

The two major effects of the interface traps, as the recombination center and the changes in the band bending at a given bias because of their charge, are modelled here. With the Trapped Charge Advanced Application Module which is an extension to MEDICI[8], we modelled the carrier trapping and de-trapping which contribute to the gated-diode current. The interface damage basically modifies this current as it affects carrier lifetime and here the trapping-detrapping process. This is the crucial feature to model the deep donor/acceptor states. It is worth mentioning that in this simulation the inclusion of the Shockley-Read-Hall Recombination Model[9,10] is mandatory. Essentially, the basic principle of the gated diode measurement[11] rests on the Shockley-Read-Hall statistics[9]. In addition, the impact of the carrier lifetime as affected by the interface trap density, N_{it}, is modelled by the effective carrier lifetime. Here, the effective lifetime for the carrier, treated as a function of the interface trap density, will take into account the changes at the SiO_2/Si interface. Hence, they will give rise to an additional recombination component at specific insulator-semiconductor interfaces due to the changes in the effective carrier lifetime. The basis of this model is that a higher trap density results in a shorter effective lifetime for the carrier[12].

Apart from this, the interface traps employed are the donor and acceptor states modelled according to the known P_{b0} centers. The donor states are centered at 0.25eV above the silicon valence band maximum and acceptor states 0.3eV below the conduction-band minimum[13]. The donor states are neutral when filled with electrons and positively charged when empty. On the other hand, the acceptor states are negatively charged when filled with electrons and neutral when empty. The effect due to P_{b1} centers[14] has been neglected for the obscurity in bandgap distribution of this trap species. In all the simulations, the fixed charge density is assumed to have a constant value of 2 X 10^{10} cm^{-2}. In the simulations, auger recombination and the dynamics of interface traps were solved self-consistently with Poisson's equation, the electron and hole current-continuity equations.

3 RESULTS AND DISCUSSIONS

A typical gated-diode current versus gate bias before stress is as shown in solid line in Fig 3.

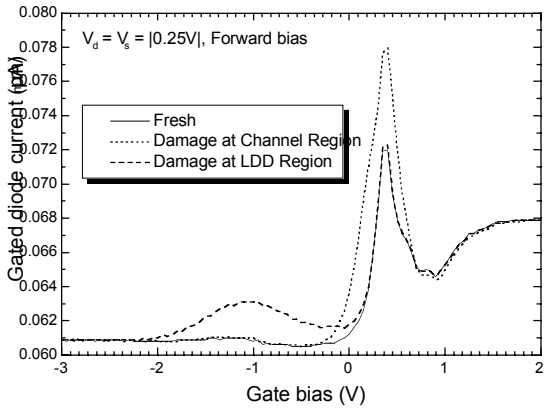

Fig 3 Gated-diode current versus gate bias due to N_{it} at either the channel region or the drain region.

The origin of the gated-diode current peak at 0.4V gate bias is due to the recombination at the centers within the channel depletion region at the interface[11]. To study the spatial effect of the damages on the gated-diode current, we have separately placed a same interface trap density of 1 X 10^{12} $cm^{-2}eV^{-1}$ at the different region of the SiO_2/Si interfaces of the MOSFET's. In the case of the light dotted line, the interface traps were placed at SiO_2/Si interfaces in the channel region terminating at the LDD-channel junction. In the case of dark dashed line, the traps were placed in the LDD region extending from LDD-channel junction at the interface. Each of these spatial distributions of the damage contributed a peak at the gate bias of 0.4V and -1.0V respectively. It must be noted that originally there has already been a peak at 0.4V gate bias as explained earlier. However, when the surface is depleted, the interface traps at the Si/SiO_2 interface provide yet another contribution to the total gated-diode current thus the increase in the peak from the original at this gate bias.

The carrier concentration distribution at the aforementioned two gate biases is shown in Fig 4 and Fig 5 respectively. From these figures, it can be seen that when the gate bias is changed, the region with equal carriers assumes different position. Specifically, the "equal carrier" region moves from the channel region to the drain region when the gate voltage is swept from positive to negative values. The carrier recombination current, which

contributes to the gated-diode current, is maximum when the electron and hole concentrations are equal. As seen in Fig 4 and Fig 5, the carrier concentration is equal in the channel and junction region at the gate-bias of 0.4V and –1.0V respectively.

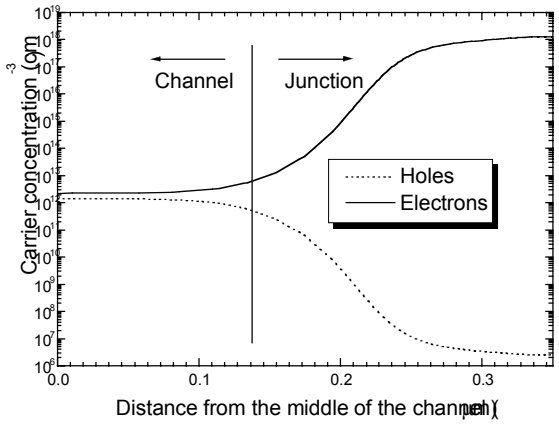

Fig 4 Carrier concentration at the MOSFET Si/SiO_2 interfaces with gate bias of 0.4V, $V_d = V_s = |0.25V|$ and $V_{sub} = 0.0V$.

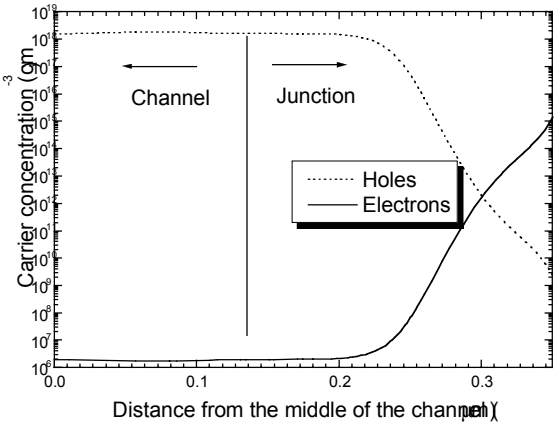

Fig 5 Carrier concentration at the MOSFET Si/SiO_2 interfaces with gate bias of -1.0V, $V_d = V_s = |0.25V|$ and $V_{sub} = 0.0V$.

It clearly shows that these different spatial distributions of N_{it} have contributed to different peaks of the gated diode current versus gate bias curve in Fig 3. In addition, the "equal carrier" length is different in the channel and drain region due to the different doping profiles in these two regions. This will also give rise to different gated-diode current. Therefore, for a continuously distributed N_{it} extending from the channel into the LDD, there will be two peaks as spatial distribution of the damages covers these two regions which will separately give rise to a peak each.

By varying the N_{it} and their respective effective lifetime, a series of the gated diode current characteristics are obtained as in Fig 6. We observe that the peak due to the channel traps is branching into two when the damage is increased. This shows that the relative strength of the different interface states clearly dominates at a certain gate bias when they are active thus giving rise to the two peaks.

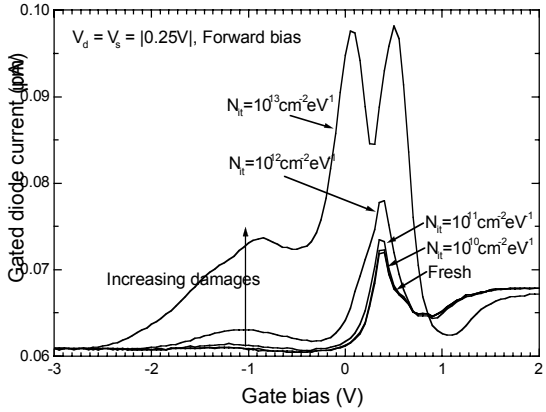

Fig 6 Gated-diode current vs gate bias with both acceptor and donor type interface traps.

The effects due to the individual species of the interface traps is investigated. Fig 7 shows the effect due to donor-type interface traps.

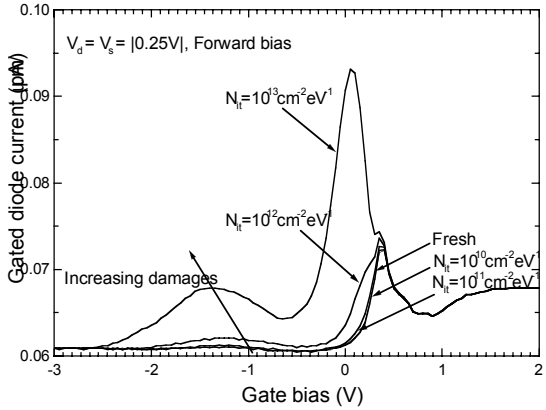

Fig 7 Gated-diode current vs. gate bias with only donor type interface states.

The donor-type interface traps, which are positively charged when empty, will result in the total positive charge at the interface. This is usually when the p-substrate is in depletion. Therefore, higher effective gate bias is required to sweep the p-substrate from inversion to accumulation and the peak is shifting to the left as the damages are increased.

Similarly, as shown in Fig 8, the acceptor-type interface traps, which are negatively charged when filled with electrons, will result in the total negative charge at the interface. Therefore, lower effective gate bias is required to

sweep the p-substrate from inversion to accumulation and the peak shifts to the right as the damage is increased.

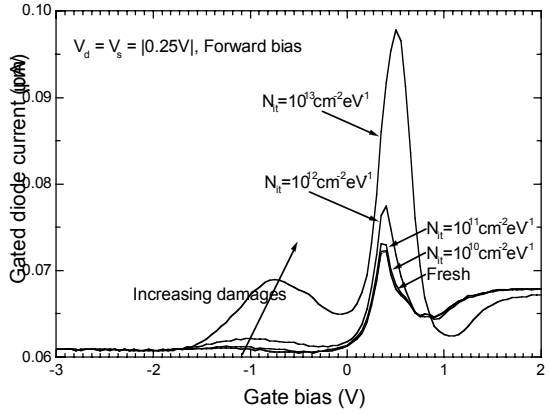

Fig 8 Gated-diode current vs gate bias with only acceptor type interface states.

It is worthwhile to note that when both of these states are present at relatively high density, due to the asymmetry of the Fermi level within the bandgap for the p-substrate and the LDD junction, the combinations of these factor gives rise to the double peak due to the channel traps as in Fig 6.

From the results, it is clear that the peak at -1V is able to yield quantitative information on the traps in the channel region. Also, the peak at 0.4V is able to yield quantitative information on the traps in the LDD region. The sensitivity of gated-diode current to changes in trap density is very good. However, the technique is not at all sensitive to the type of trap at low trap concentration levels. At high trap concentration levels, the technique is able to distinguish between the two types of traps as seen in the dual peaks of Fig 6.

4 CONCLUSIONS

Two dimensional simulations of the gated-diode diode current were presented. Its sensitivity to interface traps density in sub-micrometer MOSFET's was studied. We have to include the carrier trapping and de-trapping apart from the SRH model which is critical in modelling damage in hot carrier stressed MOSFET in the gated diode configuration. The results of simulations naturally depend on the choice of parameters. It was found that the effect of donors and acceptors at the interfaces can be modeled by a simple expression relating the carrier lifetime to the N_{it}. The peak gated diode current obtained when the effective depletion zone is at the channel will give an indication of how the channel region is damaged. It is an important guide for reliability studies in sub-micrometer MOSFET's where the high electric field moves from the drain towards the channel region.

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