Systematic Global Calibration of a Process Simulator

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ABSTRACT

This paper proposes a novel methodology of systematic global calibration of a process simulator and validates its accuracy and efficiency with application to memory and logic devices. With 175 SIMS profiles which cover the whole range of conditions of implant and diffusion processes in the fabrication lines, the dominant diffusion phenomenon in each process temperature region has been determined. Using the dual-Pearson implant model and the fully-coupled diffusion model, the calibration was performed systematically. We applied the globally calibrated process simulation parameters to memory and logic devices to predict the optimum process conditions for target device characteristics.

***Keywords*: ** Process Simulation, Calibration, Implantation, Diffusion, Silicidation

1 INTRODUCTION

Accurate and reliable TCAD (Technology Computer-Aided-Design) tools play a major role in development and manufacturing of semiconductor devices. The progress of ULSI (Ultra Large Scale Integrated Circuit) technologies to yield higher density DRAM and ultra-high performance and low power chips has brought the need to use in a wide variety of ways of TCAD tools. However, there are still many limitations in the process simulation which is not sufficiently modeled. As ULSI technology advances, the accuracy and predictive capabilities of process simulation have become more and more important in device design and development [1-2]. Furthermore, it is necessary to use the process simulation parameters which are globally applicable to all kinds of devices in fabrication. This paper proposes a novel methodology of systematic global calibration and validates its accuracy and efficiency with application to memory and logic devices.

2 METHODOLOGY

The process simulator calibration environment based on the SANTA TCAD framework [3], as shown in Fig. 1, has been constructed to systematically extract ion-implantation and diffusion model parameters. The SANTA TCAD framework (Samsung's Navigation for TCAD) worked as a manager of the database, the optimizer and runner to control the simulation status on distributed systems.

We analyze the implantation, gate oxidation and annealing process conditions of each process technology generation to make the critical point of experimental window. Based on this experimental window, we process the short-loop experiment such as in the right box of Fig. 1. The SIMS data are stored as SANTA-DB (Database) for efficient handing [4]. From the target SIMS data, we optimize the parameters which are previously determined for each process condition by the sensitivity analysis. As shown in center and left the box diagrams in Fig. 1, we sequentially extract the diffusion parameters starting from the intrinsic carrier concentration region with impurity diffusivity to TED (Transient Enhanced Diffusion) parameters. Then the set of the extracted parameters are validated using device simulation in term of electrical characteristics.

3 CALIBRATION

With 175 SIMS profiles which cover the whole range of conditions of implant and diffusion processes in the fabrication lines, the dominant diffusion phenomenon in each process temperature region as shown in Fig. 2 has been determined.

From the fully-coupled diffusion model [5], impurity diffusivities at the high temperature over 950_ and interstitial-related parameters from the OED (Oxidation Enhanced Diffusion) phenomenon at 900_ have been sequentially extracted. Then, the parameters for the impurity-defect pair movement have been extracted because the impurity redistribution and dopant activation are dominant below 850_. In addition to implant and furnace diffusion calibration, the TED (Transient Enhanced Diffusion) parameters in RTA models including the silicidation process have been extracted at the final calibration step. The adjustment of parameters for the dose loss and snow plowing effects has been considered for the whole range of temperatures.

Fig. 3 shows that the simulation results for ion-implantation with calibrated parameters are well matched to the peak and tail regions of as-implanted SIMS profiles for arsenic and phosphorus impurities. The implantation table of TSUPREM4 [6] is good for medium dose and energy, but the low energy and the high dose ranges have

discrepancy in the peak and tail profiles. Optimization is carried out using the 9-momentums of the dual-Pearson model.

Fig. 4 also shows the accurate simulation results for boron and phosphorus redistribution caused by the source and drain implantation damage at the RTA temperature and time of 975_/30sec. To monitor how the TED affects the channel impurity redistribution, the damage generation is made by high dose (5.0E15cm^{-2}) arsenic implantation which is the condition for the source/drain process. The surface concentration pile-up is the result of the gradient in the interstitial concentration produced by recombination at the silicon/oxide interface. The gradient in the interstitial concentration produces the gradient of dopant/interstitial pairs resulting in the diffusion of these pairs towards the Si/SiO_2 interface.

Fig. 5 shows the TED simulation results of the high-dose RTA process. The simulation data for the boron impurity do not match with SIMS data perfectly, but can be a sufficiently good inputs for device simulation and characterization. Also we have calibrated the fluorine effect on the boron impurity diffusion which retards the boron TED with modification of pair-reaction parameters.

The simulation for the impurity redistribution at the $CoSi_2/Si$ interface is shown in Fig. 6. The $CoSi_2$ i s generated during Co/Si reaction and its growth is induced by the diffusion of Co atoms through the silicide layer. Thus, there are no generation of interstitials and no movement of dopant in silicon. However, the dose variation at the interface is clearly observed. At the interface, the boron impurity shows strong dose loss of which amount increases as the temperature and the time increase. But for arsenic, the snow plowing effect observed at the interface is independent of the variation of the temperature and the time. In this calibration, we consider this effect as modification of segregation and trapping coefficients [7].

4 APPLICATIONS

We applied the globally calibrated process simulator parameters to memory and logic devices to predict the optimum process conditions for target device characteristics [8]. Fig. 7 shows the simulation results of the threshold voltages for a 256M DRAM nMOS transistor with less than 1% error compared to the experimental data for the various gate lengths and channel doping conditions. Fig. 8 is the process flow for CMOS logic transistors with Co silicide contacts. Fig. 9 demonstrates the TEM photography of the 0.18_ logic transistor fabricated with the optimized process conditions obtained using the proposed global calibration methodology. Based on the simulation, we can control the threshold voltage roll-off and the surface punch-through current in the n^- region. Fig. 10 shows the simulation results with errors less than 4% for the RSCE (Reverse Short Channel Effect) for 0.18_ logic devices fabricated by the RTP and Co salicide process.

5 CONCLUSIONS

In conclusion, we have constructed a systematic calibration methodology for the ion-implantation and diffusion process simulation. With 175 SIMS profiles which cover the whole range of conditions of implant and diffusion processes in the fabrication lines, the dominant diffusion phenomenon in each process temperature region has been determined. The accuracy and efficiency of the globally extracted parameters have been successfully validated in the process design of 256M DRAM and 0.18_ logic transistors. Excellent agreement between measurement and simulation of device characteristics has been achieved.

REFERENCES

[1] T. Kunikiyo, K. Mitsui, M. Fujinaga, T. Uchida and N. Kotani, "Reverse short-channel effect due to lateral diffusion of point-defect induced by source/drain ion implantation," IEEE Trans. on CAD of Integrated Circuits and Systems, Volume: 134 , 507 –514, April 1994.

[2] H. Park; M. Bafleur, L. Borucki, C. Sughama, T. Zirkle, A. Wild, "Systematic calibration of process simulators for predictive TCAD," 1997 Int. Conf. on Simulation of Semiconductor Processes and Devices (SISPAD '97), 273 –275, 1997.

[3] J. K. Park, C. H. Choi, Y. K. Park, C. S. Lee, J. T. Kong, M. H. Kim, K. H. Kim, T. S. Kim and S. H. Lee, "A characterization tool for current degradation effects of abnormally structured MOS transistors," 1997 Int. Conf. on Simulation of Semiconductor Processes and Devices (SISPAD '97), 41 -43, 1997.

[4] T. Tatsumi, H. Ohtani, S. Takahashi, S. Shimizu, M. Mukai and Y. Komatsu, "MOSQue : A Novel TCAD Database System with Efficient Handling Capability on Measured and Simulated Data," 1997 Int. Conf. on Simulation of Semiconductor Processes and Devices (SISPAD '97), 265-268, 1997.

[5] N.E.B. Cowern, M. Jaraiz, F. Cristiano, A. Claverie, and G. Mannino, "Fundamental Diffusion Issues for Deep-Submicron Device Processing," IEEE Int. Electron Device Meeting (IEDM '99), 333-336, 1999.

[6] *User's Manual of TSUPREM4 ver.1998.4,* Avant 1998.

[7] Y. Oh and D. Ward, "A Calibrated Model for Trapping of Implanted Dopants at Material Interface During Thermal Annealing," IEEE Int. Electron Device Meeting (IEDM '99), 509-512, 1999.

[8] J. H. Lee, S. W. Lee, J. T. Kong and Y. W. Kim, "Systematic Calibration for Transient Enhanced Diffusion of Indium and It's Application to 0.15um Logic Devices," 6th Int. Conf. on VLSI and CAD (ICVC '99), 53-56, 1999.

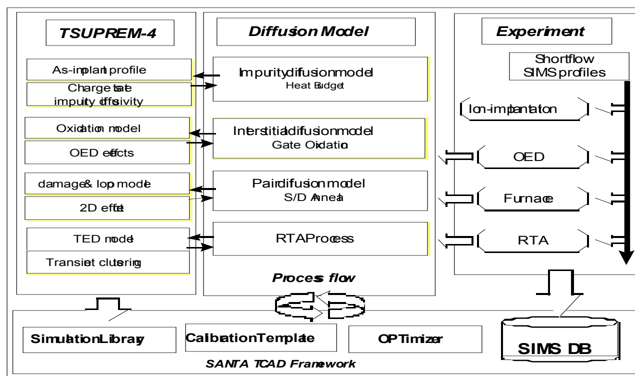

Fig. 1. A new calibration environment for a process simulator.

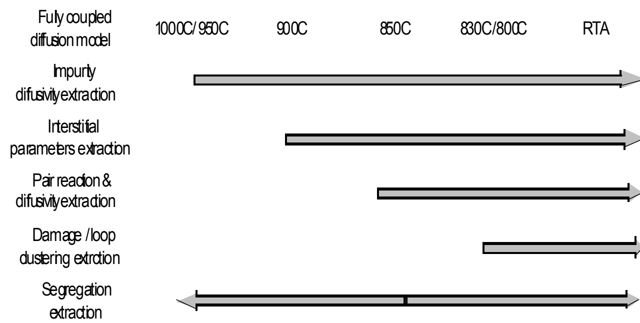

Fig. 2. The global calibration methodology for the fully-coupled diffusion model.

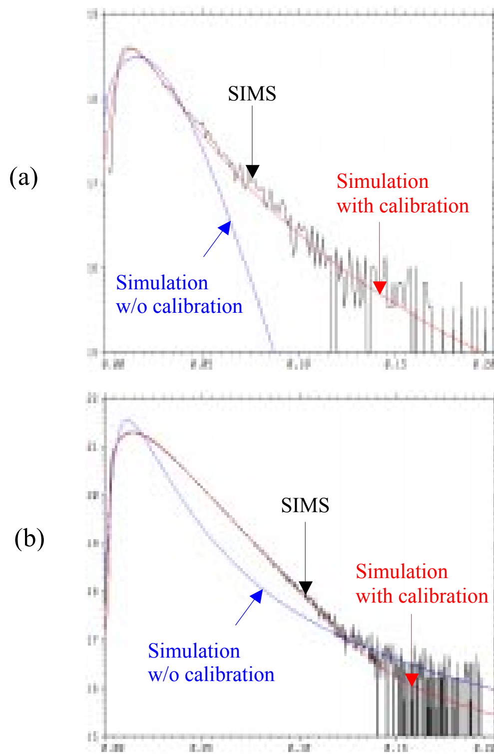

Fig. 3. The calibration results of the ion-implantation process compared with SIMS data.
(a) Arsenic impurity.
(b) Phosphorus impurity.

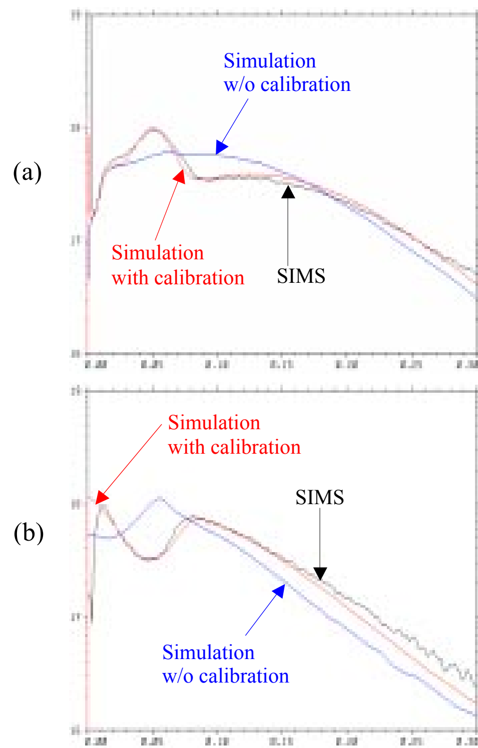

Fig. 4. Calibration results of the RTA process compared with SIMS data.
(a) 975_ 30 sec. RTA : boron impurity.
(b) 975_ 30 sec. RTA : phosphorus impurity.

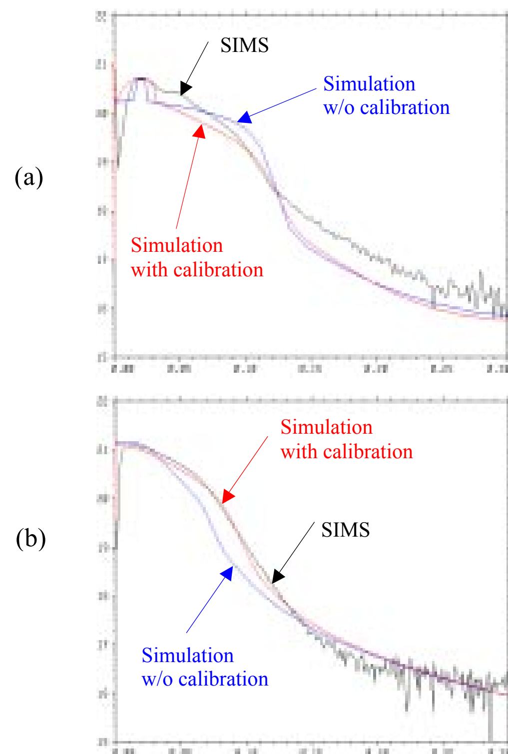

Fig. 5. Simulation and SIMS data of the RTA process.
(a) Boron impurity. (b) Arsenic impurity.

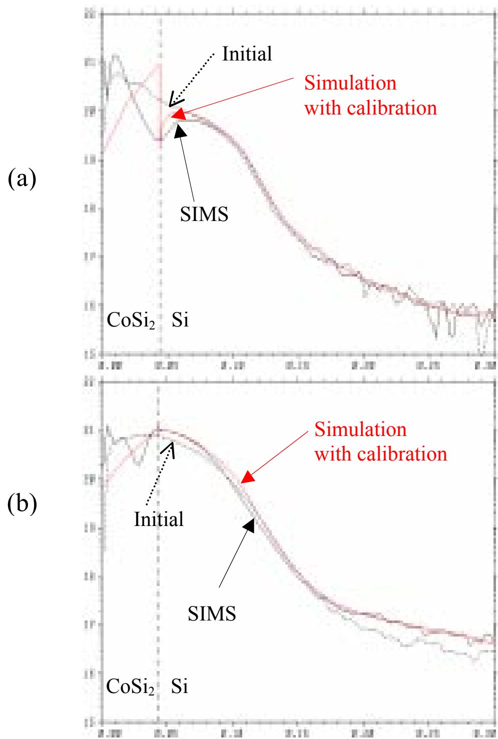

Fig. 6. Simulation and SIMS data of dopant redistribution due to the Co salicide process ($CoSi_2$ thickness=430_)
(a) Boron impurity. (b) Arsenic impurity.

- **Active photo and trench etch for STI**
- **N-well implantation**
- **Vth implantation of NMOS and PMOS**
- **Oxidation for formation of gate oxide**
- **Deposition and patterning of gate poly-silicon**
- **N- and P- source/drain implantation**
- **Formation of spacer**
- **N+ source/drain implantation and RTP anneal**
- **P+ source/drain implantation and RTP anneal**
- **Deposition of cobalt film**
- **Silicidation**

Fig. 8. The process flow of CMOS logic devices with Co-salicide contacts.

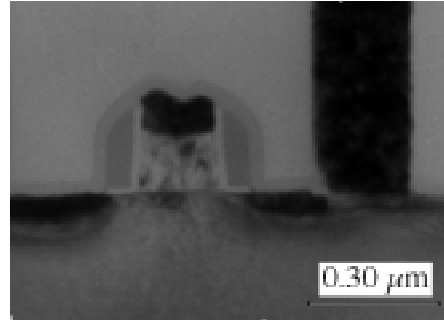

Fig. 9. The TEM photograph of 0.18_ CMOS transistor structure fabricated by the Co-salicide process (Tox=35_). new

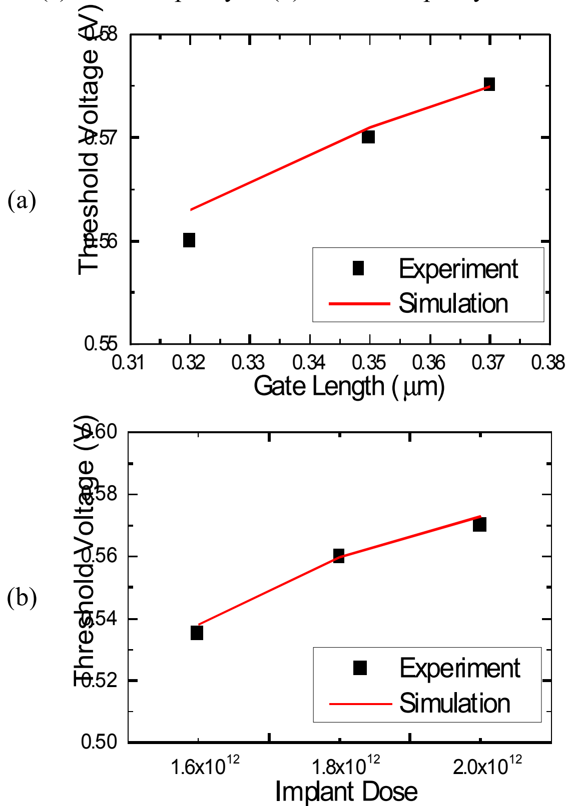

Fig. 7. The threshold voltages of a 256M DRAM nMOS transistor depending on (a) various gate lengths and (b) channel implant dose variation.

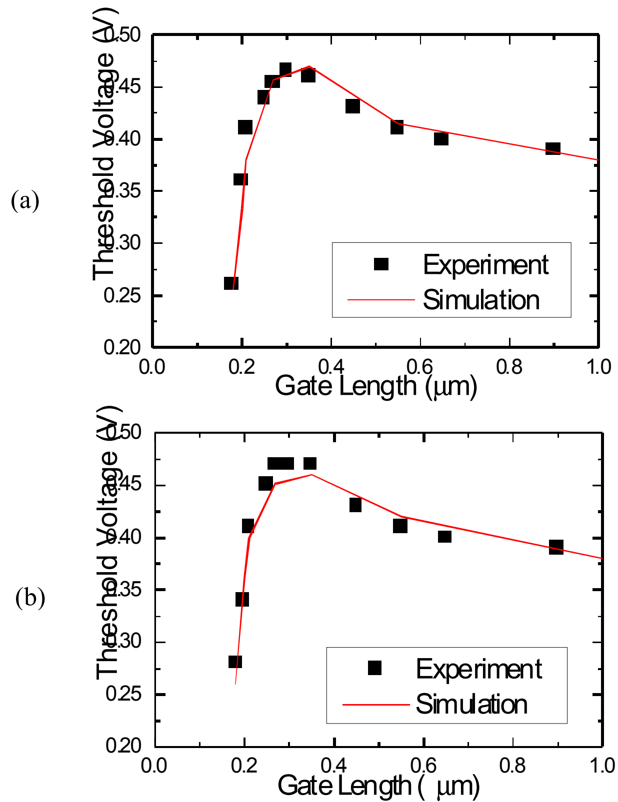

Fig. 10. RSCE simulation results compared with the experimental data for (a) a 0.18μm nMOS transistor and (b) a pocket-implanted 0.18μm nMOS transistor.