Full-chip Process Simulation for Silicon DRC

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ABSTRACT

We have developed fast IC process simulation technique based on an empirical resist and etch models to compute the silicon image of designs as large as a full ULSI chip. The simulated silicon image is used to verify the correct electrical operation of the chip and its compliance to semiconductor manufacturing rules. This significantly reduces the manufacturing and development turn-around-time (TAT) by decreasing the number of costly and time-consuming manufacturing test cycles.

The basis of these techniques is a fast edge-based optical and process simulator. An edge-movement algorithm is used to compute the displacements of edge fragments in the original design, yielding an approximation to the silicon image. In this paper we will demonstrate the need for Silicon DRC, describe the simulation and image computation algorithms, and illustrate the usefulness of the technique on real circuits.

Keywords: OPC, DRC, lithography.

1 INTRODUCTION

When feature dimensions of integrated circuits are smaller than the wavelength of the IC manufacturing process, optical and process errors are on the same order of magnitude as the feature size. As a consequence, the fidelity of the silicon image to the design suffers. Figure 1 demonstrates typical distortions for 150 nm design being printed with 248 nm laser light. Optical and Process Correction (OPC) "pre-warps" the circuit layout to counter the distortions of the optical, resist, and etch systems, resulting in features that are printed according to the design intention.

A new requirement of sub-wavelength manufacturing is the ability to ensure that optical and process errors have not violated the integrity of a design. This may, for instance, determine if OPC is necessary, or check the usefulness and correctness of OPC modifications. Mentor Graphics Calibre ORC™, Calibre OPCpro™, and Calibre PRINTimage™ modules [1] explore this field with the concept of Silicon DRC: conventional design rule checking (DRC) and layout-versus-layout (LVL) are applied to the silicon image of the layout, rather than the layout itself.

Process simulation of large chip areas is a challenging problem that received attention in the last decade with the combined employment of fast optical simulation methods (mainly the Hopkins approach), fast resist process models such as the original Cobb VTRM (variable threshold resist model) [2] and the Brunner model [3], the decomposition technique [4], and quasi-empirical modeling [5,6]. The majority of this research is driven by OPC because it requires accurate and fast process simulation of large silicon chip areas. The merging of DRC layout engines with this kind of process simulation creates many new applications in various areas of DFM (design for manufacturing) including CD control analysis, yield loss studies, and circuit performance estimations [7-9]. One class of such applications, "Silicon DRC", is described in section 3. Fast optical and process simulation methods are first described in section 2. Section 4 presents the results of these applications on a large circuit layout.

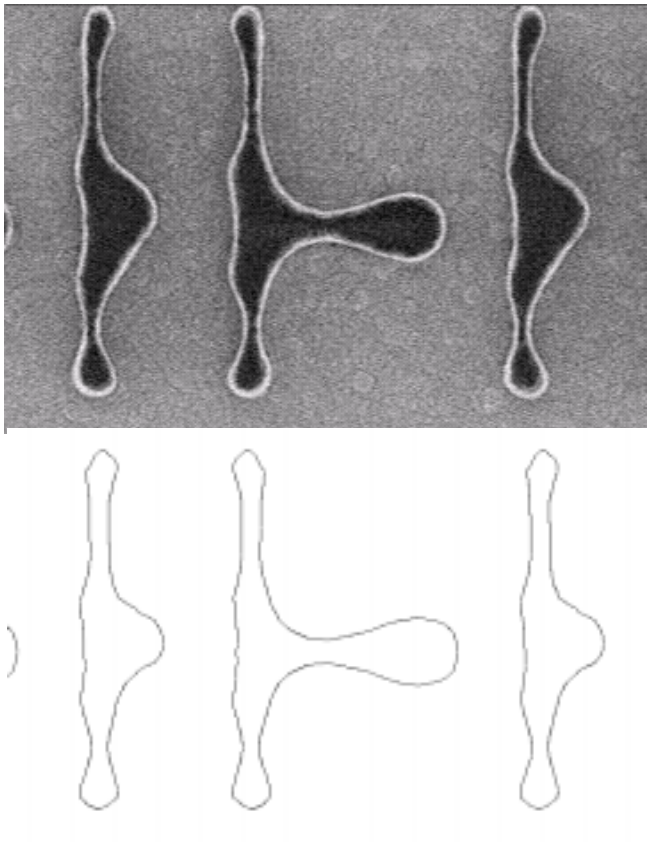


Figure 1: Simulated printed image (bottom) and correspondent SEM (top, [11]) demonstrate typical image distortions mainly caused by the optical proximity effects.

1 SIMULATION METHODS

The objective of our simulator is the determination of the printing location of an edge in a circuit layout. This

requires simulating the optical intensity at several points near the center of the edge, and using them in the process model to compute the edge formation.

The optics simulation is based on the Sum of Coherent Systems Decomposition (SOCS) method [2]. First, the Hopkins transmission cross coefficients (TCCs) are computed via aerial imaging [10]. A truncated singular value decomposition is performed on the TCC matrix to reduce computational time. The coefficients capture stepper optics - including defocus and aberration effects - and do not depend on the layout geometries.

To compute intensity at a point on a mask, the simulator evaluate the contribution of each nearby edge to the image intensity. "Nearby" edges are those that have an optical effect at the point. This simulation technique uniformly handles binary, phase-shifted and attenuated masks through complex transmission coefficients. Multiple exposures are also easily simulated.

The resist exposure and development is modeled by a variable threshold resist model (VTRM). The VTRM is a natural extension of a constant threshold resist model (CTRM). The CTRM is based on the assumption that the resist is very thin and of a very high contrast. Under these conditions the development reaction propagates strictly vertically. The original Cobb VTRM depends on 2 parameters, maximum image intensity and image slope, that account for the horizontal resist development. The model is empirically tuned to reflect the chemical properties of the resist and specifics of the manufacturing process by calibration to test patterns with typical layout shapes and pitches. The VTRM-E (enhanced variable threshold model) provides further refinement of the VTRM by explaining line end processing effects. The qualities of the different resist models are contrasted in the following table for a typical test pattern with 120 CD measurements.

Model Type	***Average CD Prediction Error, nm***	***Maximum CD Prediction Error, nm***
CTRM	15	41.8
VTRM	6.4	36.8
VTRM-E	4.3	15.4

Etch effects are modeled by fast convolution of the mask with gaussian kernels. This effectively accounts for variations in the etch reaction ratio, which is dependent on local feature density. The size of the kernels is usually twice the size of the optical diameter for modern etch processes.

The computationally complex optical simulation is made tractable in several ways. The first is an intelligent choice of spatial sampling. Rather than indiscriminately calculate the aerial image on a grid over an area, sparse computations are done only at certain critical points. These points, or "sites", are near the centers of edges whose placement errors are needed. A sophisticated syntax exists to specify the site locations to ensure sufficient detail. The number and location of sites varies depending on what flavor of simulation is required. While this method does not give an exact wafer image everywhere, it does provide enough information to identify most manufacturing problems, which almost always occur near feature edges. This sparse sampling reduces aerial image computation by an average factor of 10.

Circuit files consist of atomic units called cells which hold either geometry or other cells. Each cell may be placed any number of times in any other cell. A second major source of efficiency is the use of this design hierarchy to avoid redundant computation. Hierarchical handling becomes difficult in optical simulation due to the interactions of neighboring cells in different contexts. Naïve or straightforward hierarchy management may flatten the design excessively or produce useless results. The Selective Promotion™ and Hierarchical Injection™ algorithms of Calibre allow processing of hierarchical files with minimal degradation of the hierarchy. Depending on design type, computation savings range over several orders of magnitude.

Two applications of fast optical and process simulation are Optical Rule Checking (ORC) and wafer image simulation. In most cases, IC designers are not interested in the details of simulations, but only the consequences of deviations from the desired design. ORC flags edge fragments based on their edge placement errors (EPE). EPE is defined as the difference between the desired location of an edge and the location of the edge on the wafer. Large magnitude EPEs are considered violations of the design fidelity. The PRINTimage tool produces an approximate wafer image for the entire chip. This is accomplished by fragmenting the design edges into small segments, or "fragments". The EPE for each fragment is computed, and the edge is moved to the error location. The collection of all moved edges is a piecewise-linear contour that represents the wafer image (Figure 2).

Figure 2: PRINTimage contour compared with intended design and full wafer image.

1 SILICON DRC

The ORC and PRINTimage simulation techniques described above may be used to identify areas of a circuit layout that are difficult or impossible to properly manufacture. These "silicon DRC" violations may be detected using simulation in conjunction with DRC checks. Simple violations, such as transistor line-end pullback, are found using only ORC to flag large edge placement errors (EPEs) for particular structures. More complicated

problems, such as enclosure of contacts by poly, may require the simulation of the wafer image followed by the application of conventional DRC checks on the image. A yield analysis application based on the same techniques is presented at the end of the section.

We now describe three common silicon DRC violations, and the means of finding them using the ORC and PRINTimage tools. The violations are

- ï Transistor line-end pullback.
- ï Contact enclosure.
- ï Poly layer bridging.

Perhaps the most commonly cited proximity effect, line-end pullback is the shortening of line-ends that are too narrow to print properly (Figure 3). This effect may short out transistors by exposing the gate channel edges to the implantation step. A simple EPE check using the ORC tool will reveal problem line-ends. The computation is limited to line-ends by using standard DRC methods to pass only line-ends to the simulation step.

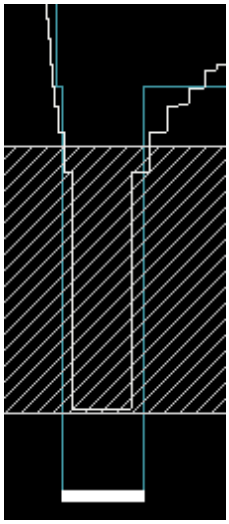


Figure 3: Line-end pullback. The original poly and active layers are shown, as well as the PRINTimage contour and the solid rectangle that identifies the bad line-end.

Contacts to the poly layer are required to lie completely within the poly layer, usually to some overlay tolerance. This type of error is detected by first simulating the images of both the contact layer and only the nearby poly. This limits the required computation. The contact image is then sized up by the desired tolerance and flagged if the result does not lie completely within the local poly image (Figure 4). Conventional DRC rules implement these last steps.

Some very close poly structures may not be resolvable, leading to the separated structures becoming connected (Figure 5). This problem may only occur away from the best process conditions, e.g., when exposure or focus are off. We examine the case when exposure varies slightly. A combination of DRC, ORC and PRINTimage steps is used to detect these violations. First, to limit simulation time, DRC steps identify proximate structures that may bridge. A fast ORC check then determines which edges are very sensitive to exposure variations. This check simulates each edge at two slightly different exposure conditions, and flags edges whose EPEs change significantly. Edges in this set are most likely to bridge, but the set may still contain false errors. The PRINTimage tools is then used to compute the image in neighborhoods around these high risk edges, to eliminate any false errors.

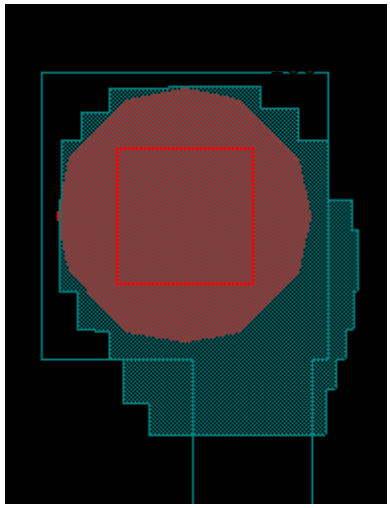


Figure 4: Enclosure violation. The original contact and poly layers are shown. The shaded layers are the oversized contact image and the local poly image. The contact layer extends slightly beyond the poly at the left.

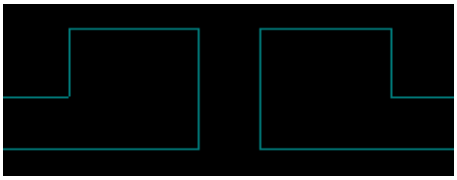
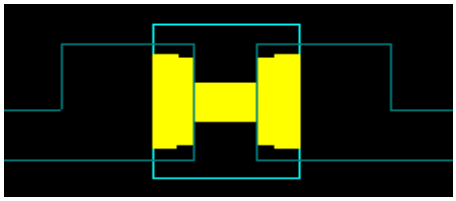


Figure 5: Bridging. The top image is the original poly.



The lower picture shows a box indicating the error, and a local wafer image demonstrating the bridge.

A combination of DRC and process simulations also provides, for the first time, an accurate direct method for CD control analysis of critical layers of the chip. We analyzed the influence of defocus on poly gate CD variation for 180 nm phase shift mask design corrected using OPC. Fine edge fragmentation is chosen to collect the simulation data of poly gate CD at 300 nm intervals along transistor channel. Figure 6 shows computed CD distributions as a function of defocus. As defocus increases, the poly gate CD variation increases. The initial bi-modal distribution splits into more modes as defocus increases, degrading device performance and thus lowering yield. A binary mask implementation of the same design, also corrected with OPC, exhibits 6 times less defocus latitude. This

demonstrates necessity of OPC *and* PSM in aggressive ULSI designs.

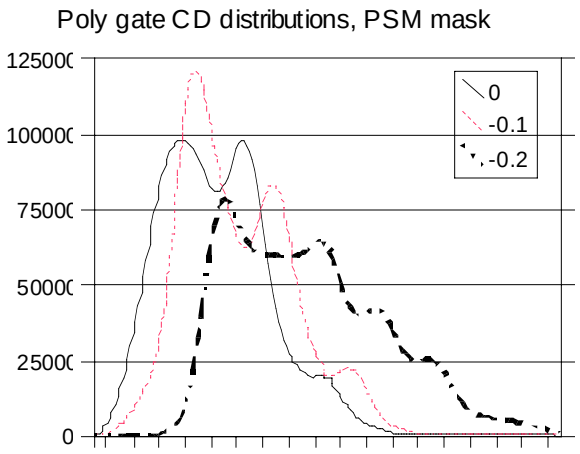


Figure 6: Poly gate CD distributions for 3 different defocuses. Computation is done over large area of logic design. CD distribution widens and shifts to the right with increase in defocus.

1 RESULTS

The three checks described above were applied to a large circuit layout. Using multiple CPUs to speed the computation, this complex job was completed in under 2 hours. Table 2 shows the numbers of errors of each type found, indicating that many problems exist in a straightforward manufacturing implementation of the chip. In reality, some form of OPC and process optimization would first be used to correct the errors and ensure manufacturability.

Error	*Hierarchical Count*	*Flat count*
LE Pullback	373094	565182
Enclosure	103	13279
Poly Bridging	7342	34951

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