Top-Down Design of MEMS

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ABSTRACT

A top-down design flow for suspended MEMS is described, starting with schematic capture of a design topology, followed by behavioral simulation, layout generation, parasitic extraction, and final verification. Support for this flow requires a MEMS hierarchical circuit representation and mapping of process, materials properties, design rules, and parasitic parameters into appropriate technology files.

Keywords: MEMS CAD, MEMS design methodology.

1 INTRODUCTION

MEMS technology has reached a critical level of maturity over the past five years, in that a system design methodology can now be put into common practice. In the context of this paper, MEMS is constrained to suspended micromechanical systems, which comprise a large variety of important applications (*e.g.*, accelerometers, gyroscopes, pressure sensors, ultrasonic and acoustic sensors, and spring-loaded microactuators). Building truly large-scale micromechanical systems with design cycles of weeks to months is becoming possible through higher levels of modular process integration, and increasing sophistication of supporting design tools. A hierarchical 'top-down' design flow starting from system concept, to components, to low-level functional elements is necessary to drive the design process directly with desired application specifications. As more engineers are trained using structured design practices that compose MEMS into smaller pieces, we will begin to see a greater quantity and diversity of mixed-domain systems-on-chip.

An example of MEMS with intermediate complexity is the multiple-resonator bandpass filter [1], which our group has adopted as one of several canonical problems to test MEMS design tools. Specifications for a such a filter include center frequency, bandwidth, passband flatness, gain, and noise. After specifications are identified, a topology is chosen, including number of microresonators, type of resonator, and type of coupling spring between resonators. By composing the system into finer blocks, eventually one reaches a level in the hierarchy that is supported with adequate models suitable for simulation. Behavioral simulation is the prime evaluation tool for determining feasibility of the chosen topology and to size elements properly.

In the last decade, designers have created primarily full-custom MEMS components by calculating and laying out each detail of the device. Over time, distinct low-level functional elements have emerged that have been reused in numerous designs. A very useful, but not comprehensive, list of these elements for electrostatically actuated, suspended micromechanical structures are beams, perforated plates, assorted flexures (*e.g.*, folded-flexure, crab-leg flexure, meander flexure, U-flexure), assorted comb-finger transducers (lateral comb drive, differential comb drive, rotary comb versions), and parallel-plate transducers. These particular elements have emerged for several reasons. Sizing can be chosen to meet functional specifications and fabrication constraints simultaneously. These elements have function that is decoupled from neighboring elements. Last, these elements can be modeled to first-order by relatively simple analytic equations.

Other elements may be included to support additional functional design spaces, such as thermomechanical sensing and actuation, or unsuspended linear and rotary structures. Occasionally, new elements will be invented, but as the technology matures, fewer innovations in low-level elements will be necessary to meet suspended micromechanical system specifications.

By providing geometric and material parameters for this small set of elements, applications can be designed through appropriate interconnection and sizing to achieve a desired functional system specification. These proven elements are commonly used for design in all lithographic-based MEMS processes, including Si DRIE and wafer bonding, SCREAM, dissolved-wafer process, CMOS-MEMS, polysilicon and thick epi-polysilicon technologies.

Our MEMS group at Carnegie Mellon is developing a design methodology for integrated MEMS that closely parallels electronic design [2]. The flow starts with a circuit schematic representation, followed by behavioral simulation for evaluation, layout generation, design rule checking, layout parasitic extraction and simulation, and ends with design verification. There are usually iterations at every part of this flow. Most of the basic CAD framework for top-down MEMS design already exists commercially. The methodology is supported within our laboratory for two integrated MEMS processes: single-layer polysilicon micromachining and 3-metal post-CMOS micromachining. In the following sections, I will provide some detail of the tools used in the flow while focusing on issues unique to integrated micromachining processes.

2 TECHNOLOGY DEPENDENCIES

One of the factors that has damped enthusiasm for top-down design is the preponderance of different processes used to create MEMS. The need for custom processing is a concern for practical use of structured design libraries and tools. For each new process, the design tool database must be populated with the appropriate materials constants, geometric dimensions, and design rules. Some of the biggest

challenges in commercialization of new MEMS fabrication technologies are characterization of material properties, metrology of structures, and the subsequent link to technology files, design rules and extraction rules. However, as this information is generated for more processes, it will become easier to use an existing, supported process and work within the layout design space (instead of process design space) to meet desired specifications.

Most of the current micromechanical device and system research at Carnegie Mellon leverages a post-CMOS micromachining process that enables low-cost integration of microstructures and CMOS electronics. Cross-sections of CMOS MEMS and Analog Devices (ADI) polysilicon iMEMS™ (also used in our research) is given in Figure 1.

To support the design flow at Carnegie Mellon, technology information must be mapped into one of four design-centric files: a layout technology file, a model technology file, a design rule file, and a layout parasitic extraction file. The MEMS layout technology file does not differ from its electronic counterpart in that it identifies the layers available for layout. Technology-dependent modeling information resides in a model technology file. The parameters for electromechanical design are nominal, minimum and maximum values for layer thicknesses, structural sidewall overetch and angles, structural release undercut, layer sheet resistance, effective material density, effective Young's modulus, residual stress, and residual stress gradient. For post-CMOS micromachining with three-metal interconnect layers, effective structural properties for 14 different beam types are needed to span the entire design space. Four of these beam types are depicted in Figure 1. Fewer parameters are required for the ADI single-structural-layer process.

Mature, practical methods exist to extract electronic properties of materials. Currently, extraction of process parameters is accomplished *ad hoc*, with much experimentation. Standardized approaches with associated test structures

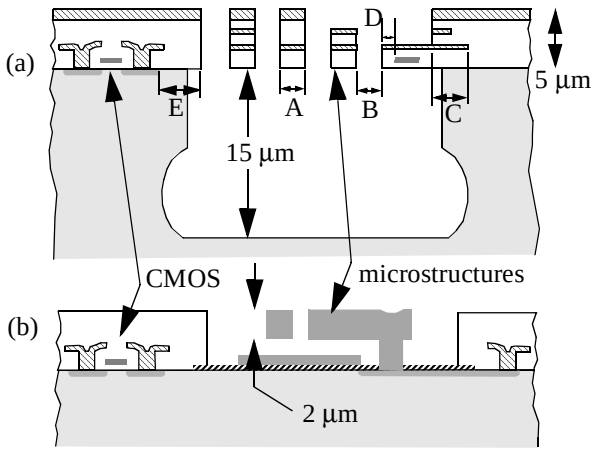

Figure 1. Examples of integrated MEMS processes. (a) Carnegie Mellon post-CMOS micromachining with design rules A to E. (b) ADI BiMOS iMEMS™. Each can share the same design flow and tools, however different geometric, material property, extraction, and design rule parameters distinguish each process.

for extraction of microstructural properties are needed to rapidly characterize processes for design tools. M-TEST [3] is one example of a methodology to extract factors related to Young's modulus and residual stress using all-electrical test. Extensions to this kind of testing methodology are sorely needed, especially for structural geometry and for residual stress gradients.

The design rule file identifies the manufacturable design space. Most of the MEMS design rules are the same as in electronic design, except the reasoning behind choosing values includes micromechanical constraints. Design rules for the CMOS-MEMS process are minimum and maximum structural width (A in Figure 1(a)), maximum beam length, minimum gap (B), minimum hole, minimum structural metal extension (C), minimum polysilicon spacing from edge (D), and minimum electronics spacing from edge (E).

The design rules are context dependent and have CMOS-MEMS specific constraints. For example, metal interconnect for electronics has a certain minimum spacing. The same metal layer, when used as a microstructural mask, has a different minimum spacing, because beam gaps are constrained by the structural sidewall etch and the ability to undercut silicon for release. Undercut for release is a non-linear function of gap and hole sizes. Picking the worst-case value for the design rule in an "one size fits all" strategy results in an unacceptable design space. Small gaps (< 3 μm) are essential for lateral actuation and sensing in low-voltage (< 10 V) CMOS processes. These transducer elements do not require wide structures (*e.g.*, comb drives have narrow fingers), however, wide structures (< 20 μm) are desirable for rigidity and wiring channels on plates. Our solution is to let minimum gap and hole size be a function of adjacent structural width.

3 BEHAVIORAL MODELING

Although element modeling is not explicitly present in a system design flow, the availability of a comprehensive set of accurate models underpins the entire design methodology. Without models, one cannot simulate and evaluate the design. Modeling of electrostatic forces, mechanics, coupled electromechanics, and damping is relatively mature, with commercial finite-element and boundary-element tools available to construct reduced-order behavioral models. Common to these model-building algorithms is the need to choose appropriate analytic basis functions and determine values through a set of numerical analyses [4][5].

Parameterized models are needed for iterative design and reuse. Physical models with geometric and material-property parameters with adequate accuracy (< 2% error) are available for a set of simple low-level elements (beams, comb drives, *etc.*). The large number of design parameters in more complex high-level components requires more simulations to produce parameterized reduced-order models. When MEMS components reach a certain level in hierarchy, models generated from finite/boundary-element tools generally become constrained to fixed parameters.

Design parameters are preserved if the higher-level components can be represented as an interconnected set of parameterized low-level elements. Behavioral modeling languages (MAST, VHDL-A, Verilog-A, VHDL-AMS) allow the models to be implemented within a variety of flexible simulation frameworks. The decoupling of the building-block elements in the design flow is the key to seamless implementation of incremental improvements in modeling.

4 MEMS CIRCUIT REPRESENTATION

In order to perform top-down design, some means must exist to define the desired microsystem concept in a hierarchical CAD representation so that one can traverse down the hierarchy to specify and verify the implementation details. The primary representations in electronic design are signal-flow (block) diagrams, network (circuit) schematics, and layout. These same representations apply to MEMS, with the addition of solid models and mesh representations for visualization and finite-element or boundary-element analysis. Ideally, automated methods would exist to seamlessly move between these five representations. In practice, manual steps are often required.

Out of the five MEMS representations, the network (or circuit) representation is the most recently developed [6][7][8]. MEMS circuit representations have direct correspondence with layout and interoperability with electronic circuits. Interconnected elements pass information via generalized through and across variables. For example, current and voltage are the through and across variables, respectively, in the electrical domain. Most MEMS circuit representations assign linear and rotational displacement as across variables and force and torque as through variables.

The gyroscope circuit in Figure 2 is designed for the ADI process and is an excellent example of the utility of design hierarchy. The central plate mass is electrostatically vibrated in x at mechanical resonance. Differential vibrations in y, induced by the Coriolis force, are sensed by detecting displacement current feeding into two transresistance amplifiers. The eight comb finger transducers near the central plate act in a parallel-plate capacitance mode to tune x and y resonance.

All of the functionality of the device is captured with only three kinds of micromechanical elements (plates, beams, and comb-finger transducers) composing the electromechanical structure. Models are written in Verilog-A for the Spectre™ behavioral simulator in the Cadence design framework. The system design of the gyroscope is completely decoupled from the effort necessary to create plate, beam, and comb-drive models.

5 BACK-END FLOW

After a design has been evaluated to meet specifications, it must pass through a series of 'back-end' steps before manufacture. These steps include layout, design-rule check, parasitic extraction and simulation, and final verification. Since the lumped MEMS circuit elements and layout have a one-to-one correspondence, layout generation is easily automated using parameterized cell layout capabilities available in commercial CAD frameworks. It is convenient to choose the same sizing parameters for both the circuit element description and the cell layout description. A pre-processor generates the absolute layout position of each element from the element size information together with the circuit netlist. This pre-processor helps eliminate redundant and error-prone data entry of position of each element by the designer. The layout position is not only required for layout generation, but is also necessary in simulation of centripetal and Coriolis forces.

For CMOS-MEMS, the increasing use of chem-mechanical polishing in sub-micron CMOS technologies necessitates slotting and filling of metal layers to eliminate dishing in open areas. Layout post-processing routines are used to automate this effort, while ensuring that the resulting fill does not affect surrounding microstructures.

Design-rule checking (DRC) executes separate electrical and mechanical rules. Since parameterized cell layout is by its nature local, element extraction from layout is necessary to ensure global correctness. Additionally, designers may customize or manually stylize the layout. Perhaps of greater importance is that context-dependent and design-dependent aspects of layout can best be recognized through extraction. An example is identification of perfect symmetry for elec-

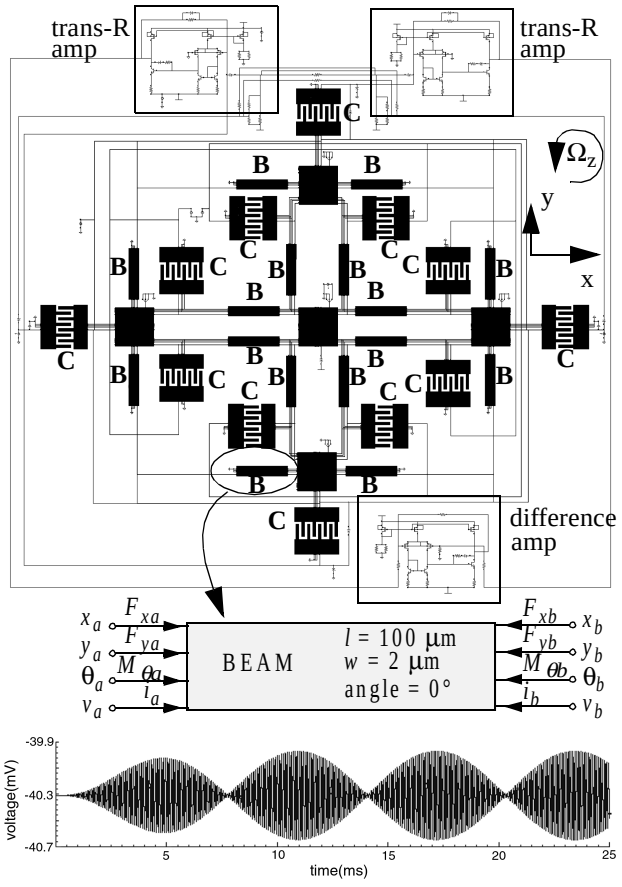

Figure 2. (a) Gyroscope schematic in the ADI process. A=plates, B=beams, and C=comb finger transducers. (b) Voltage output of the difference amp, showing a low-frequency Ω_z signal modulated with the drive frequency.

trostatic resonant systems, such as gyroscopes. It is very difficult to check manually all areas of a design for > 0.01 µm offsets, yet existence of these offsets can inject unwanted distortion into the transducer output. Automatic extraction can catch these kinds of mistakes. Another example of context-dependent DRC is detection of overlapping metal in CMOS-MEMS beams, which makes slender beams prone to lateral bending after structural release. The lateral curl is caused by layer misalignment that creates lateral stress gradients. As a last example, specific DRC for gaps may be applied to structures to improve tolerance of geometric parameters. This design technique is used on flexure beams on some commercial lateral accelerometers and in DRIE Si structures to constrain etch lag effects.

Separate design of electronics and micromechanics usually leads to system failure due to uncharacterized parasitics. Primary culprits, shown in Figure 3, are capacitive feedthrough to high-impedance (high-Z) sense nodes, resistive feedthrough via the substrate, capacitive loading on high-Z nodes, and noise from interconnect resistance. In transducers that rely on sidewall capacitance, capacitive parasitics are usually greater than the nominal sense and actuation capacitance. Capacitive parasitics of the same layout in the released microstructural area are very different from parasitics in the circuit area. The extractor must recognize the undercut microstructural areas and select critical nodes for extraction. Sidewall capacitance on these critical nodes is a first-order capacitance, not a parasitic. These extraction steps have been implemented for CMOS-MEMS in the Cadence framework. The key effort in implementation is determining the capacitance parameter values and discriminating between microstructural and electronic areas.

6 CONCLUSIONS

The top-down MEMS design methodology and hierarchical representations that parallel electronic design flow have enabled a dramatic increase in design productivity, measured in increase of manageable design complexity, decrease in time to working designs, and reduction (and eventual elimination) of number of design errors. The entire basic flow is required to provide real productivity gain; just having pieces of the design flow is not nearly as useful. Therefore, in one to two years, it is expected that full top-down MEMS design flows will be fully supported commercially. A systematic way of characterizing processes to fit into the flow is needed and is a fruitful area of future research and development.

Design verification currently requires full numerical simulation from the 3-D geometry. As MEMS behavioral models become more sophisticated, and confidence in the models increases, this verification step will migrate from evaluation with finite-element and boundary-element analysis to evaluation with behavioral simulation.

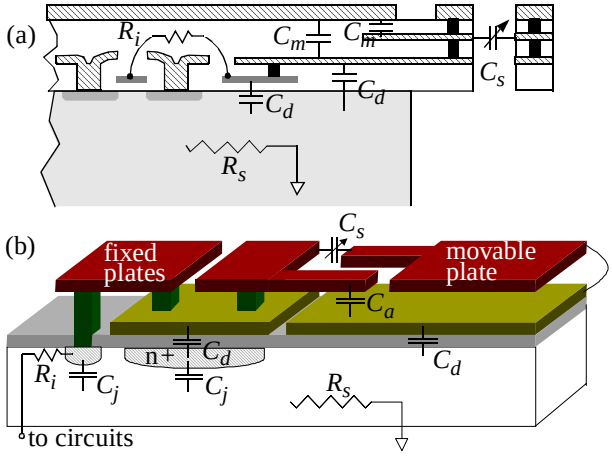

Figure 3. Capacitive parasitics in (a) CMOS MEMS and (b) iMEMS™. C_a is through fixed air-gap. C_j is junction to substrate. C_d is through dielectric to substrate or diffusion. C_m is through dielectric to metal. R_s is interconnect resistance. R_s is substrate resistance.

ACKNOWLEDGEMENT

The author thanks his graduate students. In particular, Phil Yoon has provided the results in the ADI process. Dr. Tamal Mukherjee for reviewing the manuscript and providing key insights. This research is sponsored by the DARPA MEMS and Composite CAD programs and by an NSF CAREER award.

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