Quantum Effects in SOI Devices

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ABSTRACT

Quantum effects have been reported to play an important role in the operation of narrow width SOI devices, in which the carriers experience a two dimensional confinement in a square quantum well at the semiconductor-oxide interface. This results not only in a significant increase in the threshold voltage but also in its pronounced channel width dependency. Typical method to simulate these effects is a simultaneous solution of the Schrödinger and Poisson equations, which can be a very time consuming procedure. An alternative way is to use the recently developed *effective* potential approach that takes into account the natural non-zero size of an electron wave packet in the quantized system. In this work, we have applied the effective potential approach in a recently proposed SOI device structure to quantify these effects. In a second effort we utilize the Landauer's formalism to calculate the on-state current quantum mechanically and estimate the increase in device threshold voltage due to the lateral quantization.

Keywords: SOI devices, narrow channel effect, effective potential, Landauer's formalism.

1 INTRODUCTION

1.1 Market Forces and the State of the Art

For quite some time, the dimensions of semiconductor devices have been scaled aggressively in order to meet the demands of reduced cost per function on a chip used in modern integrated circuits. There are some problems associated with device scaling, however. Critical dimensions, such as transistor gate length and oxide thickness, are reaching physical limitations. Considering the manufacturing issues, photolithography becomes difficult as the feature sizes approach the wavelength of ultraviolet light. In addition, it is difficult to control the oxide thickness when the oxide is made up of just a few monolayers. In addition to the processing issues, there are also some fundamental device issues. As the oxide thickness becomes very thin, the gate leakage current due to tunneling increases drastically. This significantly affects the power requirements of the chip and the oxide reliability. Short-channel effects (SCEs), such as drain-induced barrier lowering (DIBL) and the Early effect in bipolar junction transistors (BJTs), degrade the device performance. Hot carriers also degrade device reliability.

A solution to the above mentioned problem, in order to achieving enhanced device performance, is to use silicon-on-insulator (SOI) materials. Devices fabricated in this way are also found to be advantageous over their bulk silicon counterparts in terms of reduced parasitic capacitances, reduced leakage currents, increased radiation hardness, as well as inexpensive fabrication process. IBM launched the first fully functional SOI mainstream microprocessor in 1999 marking that SOI technology was becoming the state-of the art technology for future low-power ICs. An SOI SIMOX (separation by implanted oxygen) substrate with partially depleted epitaxial films (greater than 0.15 micron) has been used for this purpose following a 0.22-micron technology. With this effort, the IBM specifications predict a 25-35% improvement over its bulk CMOS counterpart, which is equivalent to about two years of progress in bulk CMOS design and fabrication processes [1].

1.2 Device Structures in SOI System

With regard to silicon on insulator (SOI) devices, they can be classified into two broad categories, partially-depleted (PD) and fully-depleted (FD) SOI devices. With significant number of investigations, it has been shown that FD-SOI technology has the advantages over PD-SOI technology with regard to lower junction capacitance and better subthreshold swing [2]. However, the conventional fully-depleted SOI MOSFET is known to have worse short-channel effects than bulk MOSFETs and partially-depleted SOI MOSFETs [3]. It has been shown recently that the ultra-thin body (UTB) device structure proposed by Choi *et al.* [4] and schematically shown in Figure 1 eliminates the leakage paths between source and drain. Nearly all the leakage current at $V_G = 0$ V in the $T_{Si} = 7$ nm flows along the bottom 2 nm of the body, which is least strongly controlled by the gate. Therefore, by eliminating these 2 nm, i.e. making $T_{Si} = 5$ nm can reduce the leakage by 30 times in this device structure.

It has also been reported that in both PD and FD-SOI devices there occurs a threshold voltage increase that depends upon both the impurity concentration and the SOI thickness because the inversion layer is very thin but as wide as normal gate electrode.

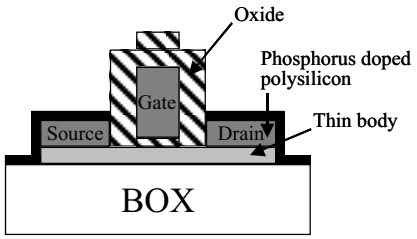

Figure 1. Schematic of an ultra-thin body SOI MOSFET.

However, in an ultra-narrow SOI MOSFET proposed by Majima *et al*. [5], schematically shown in Figure 2, the threshold voltage depends not only on the SOI thickness but also on the channel width, because horizontal carrier confinement also takes place in the narrow channel. It has been referred to this channel width dependency of the threshold voltage by quantum confinement as the quantum mechanical narrow channel effect.

Due to the experimental evidence of threshold voltage shift and the observation of Coulomb-blockade effects in the narrowest-width devices from Figure 2, it is our goal to investigate transfer characteristics of narrow-width FD-SOI MOSFETs.

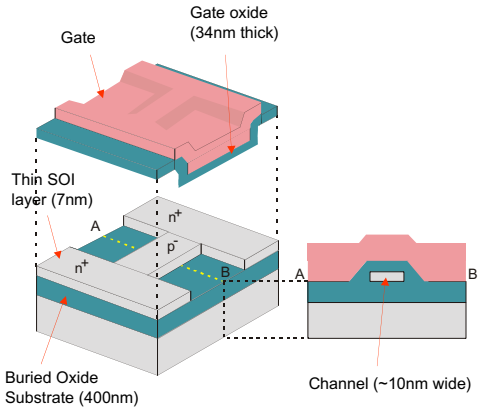

Figure 2. Device structure of ultra-narrow channel FD-SOI device structure.

1.3 Effective Potential for Device Simulation

With the scaling of devices down to nm range, it becomes challenging to approximate the quantum effects and to have device simulation tools that are able to deal with multiple levels of length scales and complexity, from the quantum regime down to the classical regime. For this purpose, increasing interest is being focused on the use of quantum mechanically derived potentials that may be added as corrections to semi-classical simulation tools. The idea of quantum potentials derives from the hydrodynamic formulation of the quantum mechanics and was first introduced by de Broglie and Madelung [6,7] and later developed by Bohm [8]. In this picture, the wave function is written in complex form in terms of its amplitude and phase $\psi(\mathbf{r},t) = R(\mathbf{r},t)\exp[iS(\mathbf{r},t)/\hbar]$. When substituted back into the Schrödinger equation it leads to coupled equations of motion that have the form of the classical hydrodynamic equations with the addition of an extra potential, often referred to as the *quantum* or *Bohm* potential, written as

$$Q = -\frac{\hbar^2}{2mR}\nabla^2 R \rightarrow -\frac{\hbar^2}{2m\sqrt{n}}\frac{\partial^2\sqrt{n}}{\partial x^2} \qquad (1)$$

where the square root of the density n, represents the magnitude of the wave function R. The Bohm potential is essentially a field through which the particle interacts with itself. It has been used, for example, in the study of wave packet tunneling through barriers [9].

In analogy to the smoothed potential representation discussed above for the quantum hydrodynamic models, it is desirable to define a smooth quantum potential for use in quantum particle based simulation. Ferry [10] suggested an *effective potential* that is derived from a wave packet description of particle motion. Within this formulation, the effective potential V_{eff} is related to the self-consistent Hartree potential V, obtained from the Poisson equation, through an integral smoothing relation

$$V_{eff}(\mathbf{x}) = \int V(\mathbf{x}+\mathbf{y})G(\mathbf{y},a_0)d\mathbf{y}\,, \qquad (2)$$

where G is a Gaussian with standard deviation a_0. This effective potential V_{eff} is then used to calculate the electric field that accelerates the carriers in the transport simulator described in more details in [11]. The use of V_{eff} has fairly low computational cost with less than 10% increase in CPU time.

2 SIMULATION RESULTS

The device structure we simulate is a narrow channel silicon on insulator (SOI) device (see Fig. 2) that consist of a thick silicon substrate, on top of which is grown 400 nm of buried oxide. The thickness of the silicon on insulator layer is 7 nm, with p^- region width between 5 and 15 nm. On top of the SOI layer sits gate-oxide layer, the thickness of which is 34 nm.

When simulating this device structure we employ two different methods:

1. The effective potential approach in parallel with the self-consistent solution of the 2D Schrödinger equation, to calculate the line electron density.

2. Use of the classical solution of the electrostatic confinement combined with the Landauer's approach to calculate the on-state current as a function of the gate voltage.

The description of these two methods and the discussion of the simulation results obtained are given below.

(A) Effective potential approach versus self-consistent solution of the 2D Schrödinger equation

When solving the 2D Schrödinger equation, we have taken into account the pronounced mass anisotropy in the Si material system and the multi-valley nature of the lowest conduction bands. Namely, the six conduction band valleys in Si are included through a standard three-valley model. Valley pair 1 points along the (100) direction having $m_x = m_l = 0.91m_0$ and $m_y = m_z = m_t = 0.19m_0$. Valley pair 2 points towards the (010) direction and has $m_x = m_z = m_t$ and $m_y = m_l$, and valley pair 3 points in the (001) direction, having $m_x = m_y = m_t$ and $m_z = m_l$. As a result of the above, at each iteration step, we solve the 2D Schrödinger equation, of the form

$$\left[-\frac{\hbar^2}{2m_y^{\nu}}\frac{\partial^2}{\partial y^2}-\frac{\hbar^2}{2m_z^{\nu}}\frac{\partial^2}{\partial z^2}+V(y,z)\right]\psi_j^{\nu}(y,z)=E_j^{\nu}\psi_j^{\nu}(y,z) \qquad (3)$$

three times, i.e. for each equivalent valley pair ν. Once the energy eigenstates and the corresponding eigenfunctions are known, the electron density is found by using

$$n(y,z)=2\sum_{\nu=1}^{3}\sum_{j}N_j^{\nu}\left|\psi_j^{\nu}(y,z)\right|^2 \qquad (4)$$

where the factor of 2 accounts for valley degeneracy, the double sum represents summation over all energy eigenstates (index j) belonging to each of the three valley pairs (index ν) and the line charge density is given by

$$N_j^{\nu}=\frac{1}{\pi\hbar}\sqrt{2m_x^{\nu}k_BT}\cdot F_{-1/2}\left(\frac{E_F-E_j^{\nu}}{k_BT}\right), \qquad (5)$$

where T is the temperature and k_B is the Boltzmann constant. In the actual evaluation of the Fermi-Dirac integral of order -1/2, which appears in Eq. (5), we use the approximate expression given in [12].

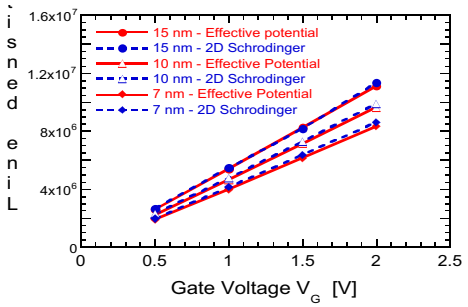

Figure 3. Variation of the line charge density for a quantum wire that represents the channel region of the SOI device structure of Fig. 2. The wire width equals 7, 10 and 15 nm.

The calculated gate-voltage dependence of the line density, for the test device structure with homogeneous confinement along the x-axis, is shown in Fig. 3. For each wire width (7, 10 and 15 nm) we use both, the effective potential approach discussed in Section 1, and the self-consistent solution of the 2D Schrödinger-3D Poisson problem. Excellent agreement is observed between the two approaches when using the theoretical value for the Gaussian smoothing parameter of 0.64 nm. This result suggests that the effective potential approach can be successfully used for more complicated confining potentials.

(B) Classical solution combined with Landauer's formalism

Another approach to modeling the SOI device is to think of it as quantum wire. This viewpoint is particularly useful in the ballistic regime, where most of the scattering comes from the device boundaries. As channel lengths become shorter, it becomes increasingly more appropriate to model devices in this manner.

A quantum wire is essentially a waveguide for propagating electron waves. Depending on the electron density and the width of the wire, only a certain number of quantized modes are allowed to propagate. The amount of current that is passed by the device then depends on the transmission probability of these modes. According to the formalism originally developed by Landauer [13] and extended by Büttiker [14], the source-drain current, I_D, can be expressed as the integral

$$I_D=\frac{2e}{h}\int\left(f(E)-f(E-eV_{DS})\right)\sum_{nm}\left|t_{nm}(E,V_{DS},V_G)\right|^2dE \qquad (6)$$

where V_{DS} is the voltage drop from source to drain, $f(E)$ is the Fermi function for energy E, and t_{nm} is the transmission amplitude going from mode n to mode m, and the summation is over all propagating modes. Thus, obtaining the current comes down to computing these quantum mechanical transmission amplitudes. There are a number of different ways for doing this, but a method that we have used with great success is that of Usuki *et al.* [15], who developed an approach based on numerically stabilized variant of the transfer matrix method. To begin, the Schrödinger equation is mapped on to a finite difference mesh on a square lattice of lattice constant a. Since the wires are of finite width, extending a given number (M) of lattice sites across, one can work in terms of slices, where ψ_j is a M-dimensional vector containing the wave function amplitudes of the jth slice. The discretized Schrödinger equation, keeping terms up to first order in the approximation of the derivative, has the form:

$$(E-\mathrm{H}_j)\psi_j+\mathrm{H}_{j,j-1}\psi_{j-1}+\mathrm{H}_{j,j+1}\psi_{j+1}=0 \quad , \qquad (7)$$

In the above equation, the $\mathbf{H}_j$ matrices represent Hamiltonians for individual slices, and the matrices $\mathbf{H}_{j,j-1}$ and $\mathbf{H}_{j,j+1}$ give the inter-slice coupling. By approximating the

derivative by finite differences, the kinetic energy terms of Schrödinger's equation get mapped onto a tight-binding model with $t = -\hbar^2/2m^*a^2$ representing nearest neighbor hopping. The potential V at site (i,j) simply adds to the on-site energies, which appear along the diagonal of the $\mathbf{H}_j$ matrices. Transfer matrices that allow translation from source to drain can be derived using (7). These allow the modes of the wire to be determined. Setting the boundary condition that these modes are occupied on the source end with unit amplitude, one obtains the transmission amplitudes that enter (6) by translating across the system. By using some clever matrix manipulations, Usuki overcame the problems created by the exponentially growing and decaying contributions of evanescent modes. Rather than just multiplying transfer matrices, the translation scheme is turned into an iterative procedure, which provides numerical stability by not allowing the evanescent contributions to diverge.

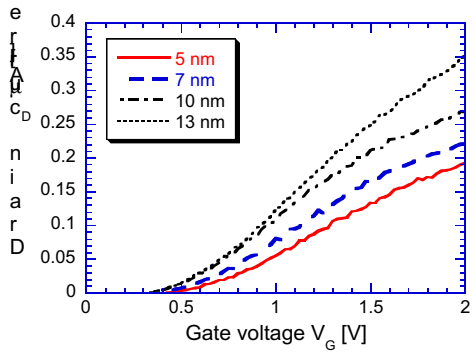

Figure 4. Transfer characteristics of the SOI device with channel width equal to 5, 7, 10 and 13 nm. The drain voltage V_D equals 10 mV.

Simulation results for the device transfer characteristics, that utilize the above described approach, are shown in Fig. 4. The channel width equal to 5, 7, 10 and 13 nm. We observe drastic decrease of the drain current with decreasing the channel width due to the lateral space-quantization effect. This observation is more clearly seen from the results shown in Figure 5, where we plot the device threshold voltage as a function of the channel width. Note that the threshold voltage equals the gate voltage for which the current equals 1 μA/μm.

3 CONCLUSIONS

In this work, we utilized the effective potential approach to successfully simulate the two dimensional space quantization effects in a model of a narrow SOI device structure. The effective potential provides a set-back of the

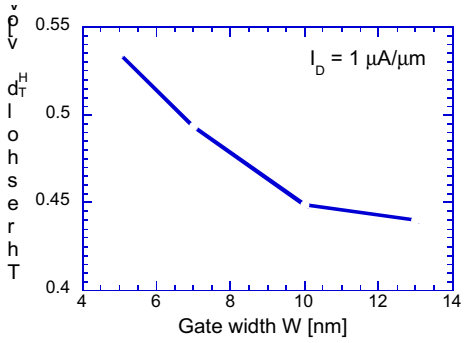

Figure 5. Threshold voltage as a function of the gate width.

charge from the interface, and a quantization energy within the channel. Both of these effects lead to an increase in the threshold voltage, which is apparent in the output characteristics of the device itself. We also found a drastic increase in the threshold voltage with decreasing the channel width.

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