In-plane and Through-plane Electrochemical Conductivity and Fuel Cell Performance of Thin-film YSZ Electrolytes

A. C. Johnson* and S. Ramanathan**

Harvard University School of Engineering and Applied Sciences
Cambridge, MA, USA
*acjohns@fas.harvard.edu, **shriram@seas.harvard.edu

ABSTRACT

We report in-plane and through-plane conductivity measurements of dense YSZ films varying in thickness from 20 to 200 nm. In-plane measurements were performed on YSZ films grown on silicon wafers coated with SiO_2 or Si_3N_4. Micro-fabricated strips with Pt electrodes in various geometries were used to obtain conductivity as a function of temperature from 200 – 600 °C in a custom-designed micro-probe station. These films have activation energies, which vary from 0.77 to 1.09 eV. Their absolute conductivity is lower compared with other reports. Through-plane and fuel cell measurements were performed by depositing YSZ on a nitrided silicon wafer, then etching through the wafer and depositing porous platinum electrodes on both sides [6,7]. We discuss the electrochemical conduction studies in detail along with fuel cell performance and correlation with electrode microstructure.

Keywords: nanoionics, solid oxide fuel cells

1 INTRODUCTION

Intermediate temperature solid oxide fuel cells (IT-SOFCs) have garnered substantial interest for small scale, environmentally friendly, portable electricity generation. Submicron electrolyte films are a key component of IT-SOFCs, using decreased thickness to compensate for increased ionic resistance at lower temperatures. In addition to their relevance to this application, several groups have reported size-dependent in-plane ionic conductivity in thin films of yttria-stabilized zirconia (YSZ) and gadolinia-doped ceria (GDC) [1-5]. Here we report both in-plane and through-plane conductivity measurements of dense YSZ films varying in thickness from 20 to 200 nm. These measurements were performed in a custom-built probe station that exposes the top side of a chip to air and, for fuel cell measurements, exposes the bottom side to forming gas. In-plane impedance spectroscopy measurements were performed on YSZ films grown on silicon wafers coated with SiO_2 or Si_3N_4 with thicknesses ranging from 20 to 200nm. Both the YSZ electrolyte and the porous Pt electrodes were patterned by optical lithography, using several geometries in order to span a wide temperature range (200 – 600 °C) as well as to investigate possible size effects or electrode contributions to the conductivity. Observed activation energies vary from 0.77 to 1.09 eV. Through-plane and fuel cell measurements were performed by depositing 40-100nm of YSZ on a nitrided silicon wafer, then etching through the wafer and sputtering porous platinum electrodes on both sides [6,7].

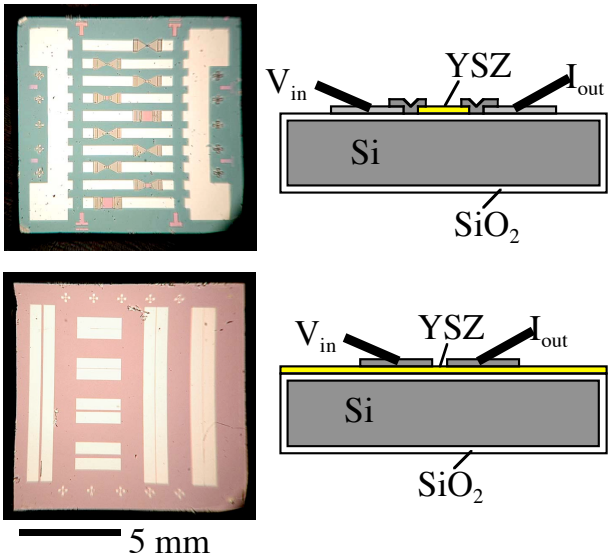

Figure 1 – Chips for in-plane measurements

2 EXPERIMENTAL

Electrical measurements, both AC impedance spectroscopy and DC fuel cell measurements, were performed on a probe station designed and built in house. A stainless steel body, around which a band heater is fitted, allows heating 1 cm samples to 600°C. Samples are sealed over a hole on top of this body with a gold gasket and clamped down by a ring on top. For fuel cell measurements, forming gas is supplied to the back side of the sample, first flowing it through a coil of tubing to thermalize it, then releasing it directly to the back of the sample. Micromanipulator probes contact individual devices on the top side, and a thermocouple next to the sample measures and controls temperature.

Figure 1 shows the two chip designs used for in-plane measurements of thin-film YSZ electrolytes. Both designs begin with silicon chips coated with approximately 1 μm of thermally grown silicon oxide, to insulate the electrodes

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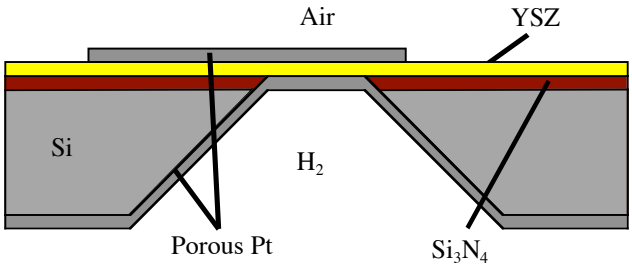

Figure 2 – Schematic of fuel cell device

from the conductive silicon chip. In the first design, rectangles of YSZ were deposited (pink) by sputtering an oxide target. Contact pads of dense Pt with a Ti adhesion layer were added (light grey), followed by electrodes of porous Pt (dark grey) with a thickness of approximately 100 nm. All patterning was done by liftoff. The result was squares of exposed YSZ ranging in size from 20 to 500 μm on a side. In the second design, a blanket coating of YSZ was sputtered onto the oxidized chip, followed by pairs of porous Pt strips, 2 and 8 mm in length, separated by gaps of 10 to 200 μm.

Similar chips were made using 200 nm of LPCVD silicon nitride as the insulator, in an attempt to determine whether the bottom interface with an oxide plays a role in nanoscale ionic conductivity. However, this insulating coating showed complex behavior in impedance spectra at high temperatures even when not connected to YSZ, so we were not able to isolate the electrolyte contribution. Instead, several chips of the first design had a thin layer of sputtered silicon nitride directly underneath the YSZ rectangle.

Figure 2 shows the fuel cell device schematically. Fabrication is similar to ref. [7]. A silicon wafer, nitrided on both sides, is blanket coated on top with a thin YSZ film, then patterned with a porous Pt electrode on top for the electrode and an etch mask (holes in the nitride) on the bottom. We etch through the silicon with KOH, which leaves pyramidal wells and stops at the nitride, then dry etch away the nitride on the bottom and on the underside of the active electrolyte area. Finally, the bottom side of the chip is coated in porous Pt to form the anode. Each chip contains six devices, with square active areas ranging from 80 to 500 μm on a side. The cathode of each device is contacted individually, while the anodes are all connected simultaneously to the body of the probe station through the gold gasket.

3 RESULTS AND DISCUSSION

In-plane devices fabricated on insulated but conductive substrates show large capacitance to the substrate, hence the impedance spectra of these devices, shown for example in Fig. 3(A), consist of single semicircles with essentially temperature-independent capacitance. Figure 3(B) shows temperature dependence of conductivity measured on a

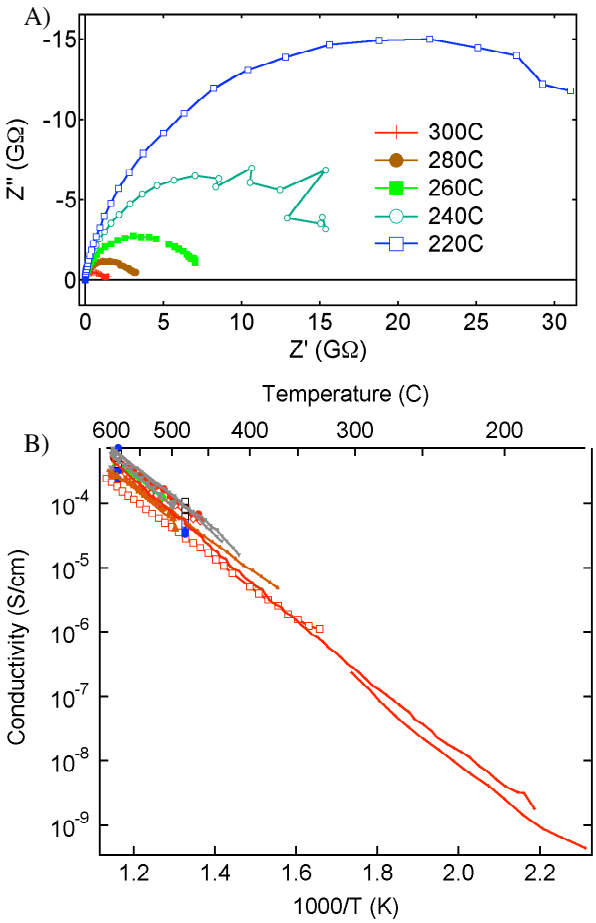

Figure 3 – A) Representative impedance spectra and B) collected conductivity data for in-plane devices

broad collection of in-plane devices, with between 20 and 200 nm of YSZ grown on either SiO_2 or Si_3N_4 and using either chip design. Some annealing was observed in initial heating, so we present data taken only while decreasing temperature from the maximum of approximately 600 °C. The activation energies extracted from these data vary from 0.77 to 1.09 eV.

Fuel cell devices were measured by supplying a mixture of 5% hydrogen and 95% argon to the underside of the chip. Open circuit voltage ranged from 0.9 to 0.94 V, showing the electrolyte to be free of gaseous or electronic leaks, and peak power produced was ~ 2 mW/cm^2 at 500 °C. Electron micrographs of similar fuel cell devices at various stages of Pt annealing, shown in Fig. 4, imply that the reason for the modest power output is poor contact between the center and edge of the anode, so that only the very edge of the device is active. Impedance spectroscopy measurements corroborate this hypothesis, showing electrolyte resistance far larger than expected from in-plane measurements but still substantially less than the electrode contribution.

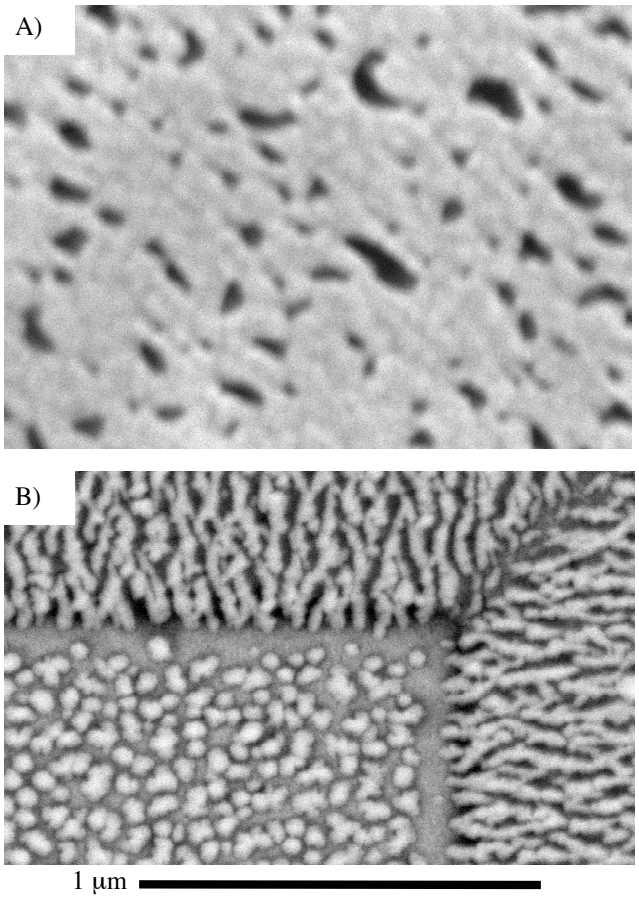

Figure 4 – Anode microstructure. A) Center of anode, shows porous but fully connected platinum. B) At the edge, however, platinum forms small grains, giving way to a gap with no connection to the platinum coating the sloping sidewalls of the silicon wafer.

4 CONCLUSION

We have successfully measured ionic conductivity at low temperatures in ultra-thin YSZ membranes through micro-fabricated devices. Preliminary results on fuel cells fabricated with Pt electrodes show power density of the order of few mW/cm^2. This is likely due to un-optimized electrode microstructure. Further work is on-going to improve electrode performance as well as understand impedance response of fuel cell devices fabricated on silicon-based substrates.

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