Novel FD SOI Devices Structure for Low Standby Power Applications

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ABSTRACT

In this paper, full-depleted SOI devices with source/drain extension shift and high-κ offset spacer were investigated in detail. The calculated results show that the source/drain extension shift can decrease off-state leakage current I_{off} significantly by utilizing the extra electron barrier height in source/drain extension shift region to reduce standby power dissipation. However, the on-state driving current I_{on} is also sacrificing simultaneously. In order to overcome this drawback, the high-κ offset spacer is used to increase the on-state driving current I_{on} effectively due to the enhanced vertical fringing electric field to elevate the channel voltage drop and reduce series resistance. Consequently, a nanoscale FD SOI device with 8-nm S/D extension shift and TiO_2 offset spacer can possess high driving current I_{on} and ultra-low leakage current I_{off} about 0.003 times lower than conventional SOI structure.

Keywords: Silicon-on-insulator (SOI), S/D extension shift, high-κ offset spacer dielectric, fringing electric field.

1 INTRODUCTION

High-performance and low-power transistors with high on-state driving current I_{on} and low off-state leakage current I_{off} are required for state-of-the-art CMOS technology [1]. Full-depleted silicon-on-insulator (FD SOI) devices have been anticipated to play a significant role for next generation technology. According to International Technology Roadmap for Semiconductors (ITRS) [1], the 65-nm node SOI processes with 32-nm channel length and 12-Å oxide thickness could be the mainstream CMOS technology. Until now, lots of efforts have been devoted to it in recent years [2]-[6]. For nanoscale MOSFETs, standby leakages current I_{off} has become serious challenges to the reliable circuit design. However, high on-state driving current I_{on} and low off-state leakage current I_{off} would not be obtained simultaneously. Therefore, a novel technology for achieving this target is required urgently. Here, we find that the source/drain (S/D) extension shift away from the gate edge can provide an extra electron barrier height to decrease the off-state leakage current I_{off}. However, this method will result in an ultra-high series resistance when device operates in on-state to degrade the on-state driving current I_{on}. In order to improve the on-state driving current I_{on}, many high-κ materials are employed widely as the gate dielectric to increase the gate capacitance [7]-[9]. Recently, high-κ material has been used as the offset sidewall spacer dielectrics to improve the on-state driving current I_{on} for the thin-film transistors (TFTs) [10][11]. In the same way, we can utilize S/D extension shift to reduce the off-state leakage current I_{off} and to improve the on-state driving current I_{on} by using high-κ offset sidewall spacer.

In this paper, the 65-nm node SOI devices with different S/D extension shifts and offset sidewall spacer dielectrics are studied by two-dimensional (2-D) device simulator MEDICI [12]. Finally, the optimized structure is derived to obtain the high on-state driving current I_{on} and ultra-low off-state leakage current I_{off} simultaneously.

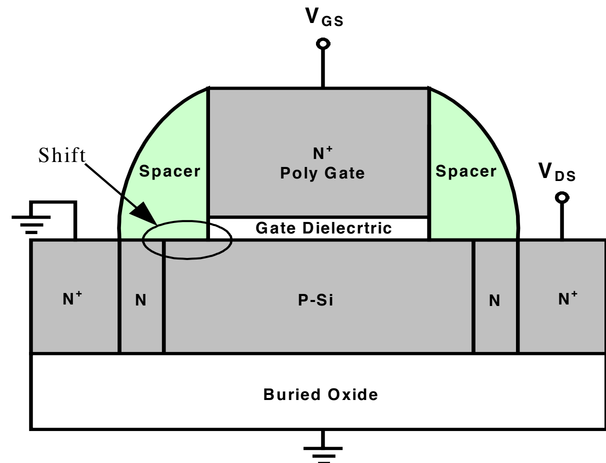

Figure 1. The FD SOI device structure with shifted source/drain extension.

2 SIMULATION PROCEDURE

Nanoscale SOI device structure used in MEDICI simulation is with a channel length of 32-nm, gate oxide thickness of 12-Å, offset sidewall spacer width of 30-nm, and body thickness of 15-nm [1][6], respectively. Five shifts in S/D extension from the gate edge, -5, 0, 5, 10 and 15-nm are used to investigate the off-state leakage current I_{off}. In order to utilize fringing electric field to improve the on-state driving current I_{on}, different dielectric constant (κ) of the offset spacer on the fringing electric field of the device, including air (ε_r=1), SiO_2 (ε_r=3.9), Si_3N_4 (ε_r=7.5), HfO_2 (ε_r=25) and TiO_2 (ε_r=80), were used. Note that the

width of spacer was fixed at 30-nm in the simulation [6].

3 RESULTS AND DISCUSSION

Figure 1 shows the FD SOI device structure with a shifted S/D extension. This shifted S/D extension results in a significant decrease of the off-state leakage current I_{off}, i.e. V_{GS}=0V and V_{DS}=1.0V, as shown in Fig. 2. Figure 2 indicates a great reduction in the off-state leakage current I_{off} by several orders with widened shift- width. It is because the shifted S/D extension region yields a extra p-type region outside the gate edge to provide a much lower surface channel potential, as shown in Fig. 3, to increase the electron barrier height, resulting in reducing the off-state leakage current I_{off}. This electron barrier height is significantly increased with the widened S/D extension shift, resulting in a progressive reduction of the off-state leakage current I_{off} as shown as Fig. 2.

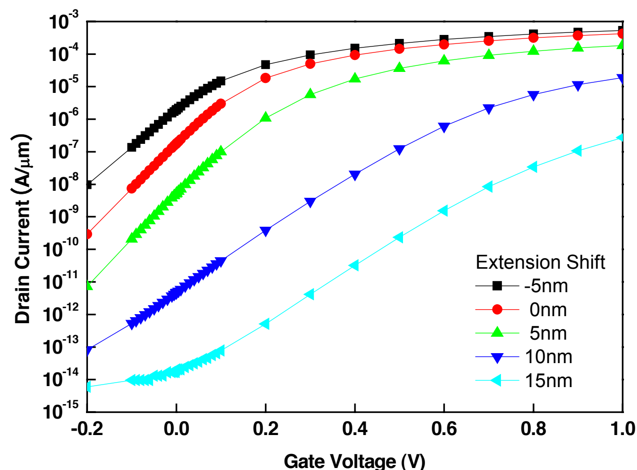

Figure 2. The I_{DS}-V_{GS} curve with different source/drain extension shift.

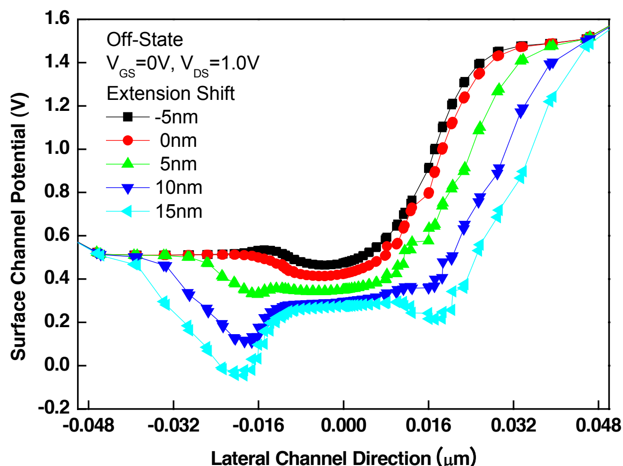

Figure 3. The surface channel potential with different source/drain extension shift in off-state.

However, Fig. 2 also indicates that the degradation in the on-state driving current I_{on}, i.e. V_{GS}=1.0V and V_{DS}=1.0V, happens simultaneously with the widened S/D extension shift. This degradation of the on-state driving current I_{on} has many accounts. The dominant account is that the widened S/D extension shift introduces a series resistance $R_{S/D}$ because of the extra p-type region. This extra p-type surface region could be inverted by the assistant of the vertical fringing electric field via the offset sidewall spacer.

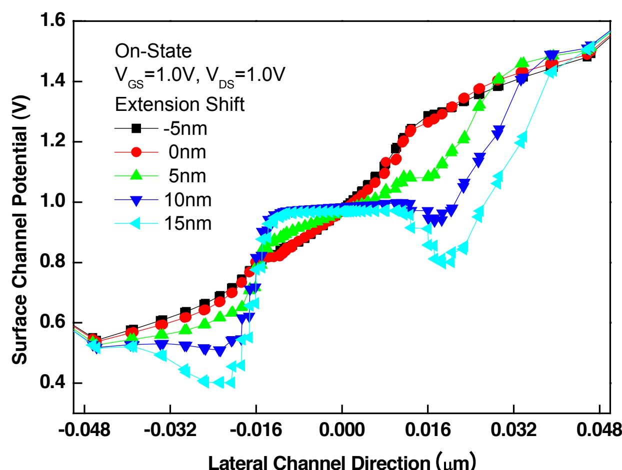

Figure 4. The surface channel potential with different source/drain extension shift in on-state.

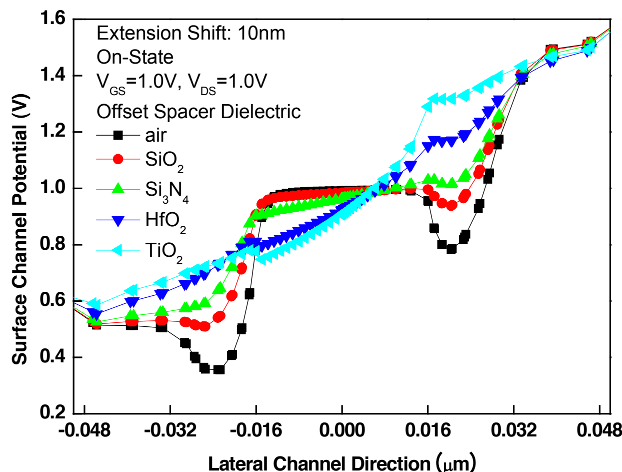

Figure 5. The surface channel potential with 10nm extension shift and different high-κ offset spacer in on-state.

The inversion layer in shifted S/D extension region maybe not formed as the extra p-type region is too wide or the vertical fringing electric field is too weak to introduce enough minority carriers. Therefore, the devices would turn on difficultly when the S/D extension shift is over 10-nm as shown in Fig. 2. Therefore, we can expect that this introduced electron barrier height could not be surmounted as the devices are in on-state as shown in Fig. 4. Figure 4

apparently indicates that two electron barrier heights exist in S/D extension shift region as the shift is over 10-nm.

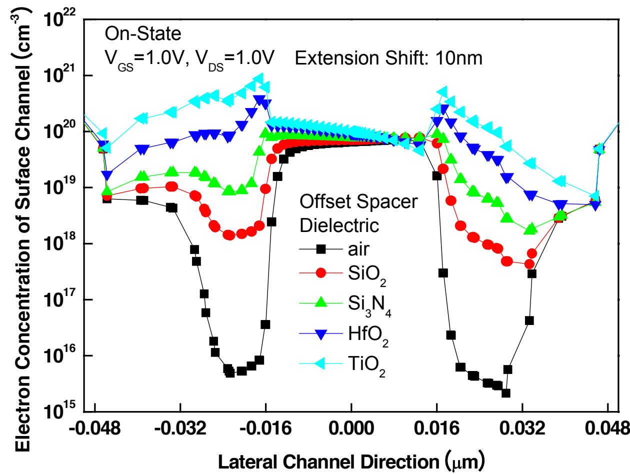

Figure 6. Electron concentration of surface channel with different spacer dielectrics in on-state region.

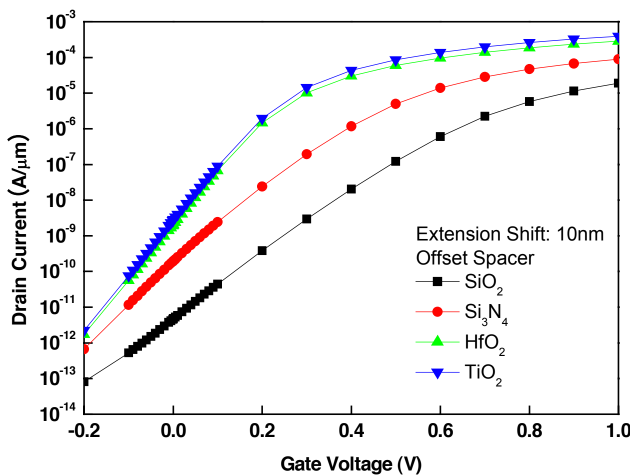

Figure 7. The I_{DS}-V_{GS} characteristics of four dielectric offset spacer SOI devices.

Although the off-state leakage current I_{off} and on-state driving current I_{on} decrease at the same time, the reduction magnitude of on-state driving current I_{on} is not as much as off-state leakage current I_{off} when the shifted width is below 10-nm. To optimize devices' performance, one can try to improve the slight degradation in on-state driving current I_{on} and maintain much lower off-state leakage current I_{off} by adopting suitable shift-width. As mentioned above, high-κ materials are used as the offset sidewall spacer dielectrics to enhance this vertical fringing electric field. Consequently, using the high-κ spacer to enhance the vertical fringing electric field for an improved on-state driving current becomes the most feasible approach. Figure 5 shows the surface channel potential with fixed 10-nm S/D extension shift and different high-κ offset sidewall spacers in the on-state. With the offset sidewall spacer dielectric constant increasing, the vertical fringing electric field was significantly enhanced to elevate the surface channel potential, resulting in reducing the electron barrier height in S/D extension shift region efficiently as shown in Fig. 5. Moreover, this enhanced vertical fringing electric field can increase the voltage drop across the surface channel and induce more minority carriers in the S/D extension shift region, including S/D extension region, to ensure the complete inversion of the extra p-type region and reduce the series resistance significantly as shown in Fig. 6.

Figure 7 shows the I_{DS}-V_{GS} characteristics of different offset sidewall spacer dielectrics. It indicates a great improvement of on-state driving current I_{on} and subthreshold swing by using high-κ dielectric as offset sidewall spacer. Similarity, the off-state leakage current I_{off} is also degrading with the increasing of on-state driving current. However, it is still useful as both technologies of high-κ offset sidewall spacer and shifted S/D extension are collocating. For an ultra-low off-state leakage current I_{off} with constant high on-state driving current I_{on} design requirement, a 8-nm shift of S/D extension shift region with TiO_2 high-κ offset sidewall spacer device can perform. Consequently, a nanoscale FD SOI device with 8nm S/D extension shift and TiO_2 offset spacer can possess high on-state driving current I_{on} and ultra-low off-state leakage current I_{off} about 0.003 times lower than conventional SOI structure is derived as shown in Fig. 8.

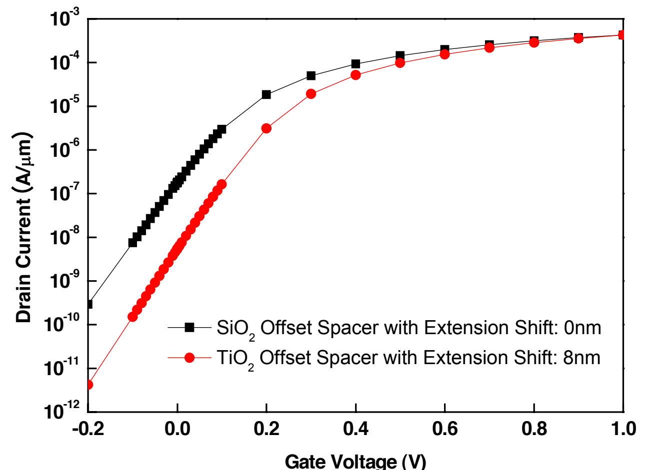

Figure 8. The I_{DS}-V_{GS} characteristics of SiO_2 spacer with zero extension shift and TiO_2 offset spacer with 8nm extension shift, respectively.

4 CONCLUSIONS

A novel nanoscale FD SOI structure possesses ultra-low off-state leakage current I_{off} and keeps high on-state driving current I_{on} is proposed for the first time. It utilizes the shifted S/D extension region to provide an extra electron barrier height to reduce off-state leakage current I_{off}. In addition, high-κoffset sidewall spacer is used to elevate the

voltage drop across surface channel and reduce series resistance to improve on-state driving current I_{on} significantly. This method provides a feasible approach to achieve both low standby current I_{off} , while maintaining high driving current I_{on} simultaneously. Consequently, a 65-nm node FD SOI device with 8-nm S/D extension shift and TiO_2 offset spacer can possess high on-state driving current I_{on} and ultra-low off-state leakage current I_{off} about 0.003 times lower than conventional SOI structure. This structure is one of the promising devices to be considered for next generation devices or beyond.

5 ACKNOWLEDGEMENT

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